EE2000: LOGIC CIRCUIT DESIGN

Effective Term
Semester B 2023/24

Part I Course Overview

Course Title
Logic Circuit Design

Subject Code
EE - Electrical Engineering
Course Number
2000

Academic Unit
Electrical Engineering (EE)

College/School
College of Engineering (EG)

Course Duration
One Semester

Credit Units
3

Level
B1, B2, B3, B4 - Bachelor's Degree

Medium of Instruction
English

Medium of Assessment
English

Prerequisites
EE1001 Foundations of Digital Techniques (only applicable to EE students)
or
EE1002 Principles of Electrical Engineering (only applicable to ITME students)

Precursors
Nil

Equivalent Courses
Nil

Exclusive Courses
Nil

Part II Course Details

Abstract

The aim is to provide students with an understanding of the concepts and design of logic circuits, including (i) various devices, techniques for analyzing and designing combinational circuits and sequential circuits, circuit design and implementation techniques, and (ii) Hardware Description Language (HDL) modelling and synthesis of combinational and synchronous sequential circuit, circuit implementation with FPGA devices. The electrical characteristics of selected logic families are also covered.

Course Intended Learning Outcomes (CILOs)

	CILOs	Weighting (if app.)	DEC-A1	DEC-A2	DEC-A3
1	Apply different methods to simplify combinational logic functions and sequential machines			x	
2	Analyze and design combinational and synchronous sequential circuits		x	x	
3	Identify electrical characteristics of different logic families		x	x	
4	Design logic circuit using VHDL Hardware Description Language		x	x	
5	Implement logic circuits with Xilinx FPGA		x	x	
6	Apply basic theories to practical work		x	x	

A1: Attitude
Develop an attitude of discovery/innovation/creativity, as demonstrated by students possessing a strong sense of curiosity, asking questions actively, challenging assumptions or engaging in inquiry together with teachers.

A2: Ability
Develop the ability/skill needed to discover/innovate/create, as demonstrated by students possessing critical thinking skills to assess ideas, acquiring research skills, synthesizing knowledge across disciplines or applying academic knowledge to real-life problems.

A3: Accomplishments
Demonstrate accomplishment of discovery/innovation/creativity through producing /constructing creative works/new artefacts, effective solutions to real-life problems or new processes.

Teaching and Learning Activities (TLAs)

	TLAs	Brief Description	CILO No.	Hours/week (if applicable)
1	Lecture	Explain keys concepts such as binary code, logic circuit, combinational and sequential circuit.	1, 2, 3, 4, 5	3 hours/week
2	Tutorial	Discuss and practice how to use the lecture materials in real implementations through the tutorial questions.	1, 2, 3, 4, 5	1 hour/week

3	Laboratory	Identify, design, and apply the fundamental logic circuits to practical work using Hardware Description Language (VHDL) and Xilinx FPGA chip.	1, 2, 3, 4, 5	3 hours/week for 5 weeks

Assessment Tasks / Activities (ATs)

	ATs	CILO No.	Weighting (%)	Remarks (e.g. Parameter for GenAI use)
1	Tests (min.: 2)	1, 2, 3, 4, 6	30	
2	#Assignments (min.: 3)	1, 2, 3, 4, 6	10	
3	Lab Exercises/Reports	4, 5, 6	10	

Continuous Assessment (%)

50

Examination (%)

50

Examination Duration (Hours)

2

Additional Information for ATs

Remark:
To pass the course, students are required to achieve at least 30% in course work and 30% in the examination. Also, 75% laboratory attendance rate must be obtained.

may include homework, tutorial exercise, project/mini-project, presentation

Assessment Rubrics (AR)

Assessment Task

Examination

Criterion

Achievements in CILOs

Excellent (A+, A, A-)

High

Good (B+, B, B-)

Significant

Fair (C+, C, C-)

Moderate

Marginal (D)

Basic

Failure (F)

Not even reaching marginal levels

Assessment Task
Coursework

Criterion
Achievements in CILOs

Excellent (A+, A, A-)
High

Good (B+, B, B-)
Significant

Fair (C+, C, C-)
Moderate

Marginal (D)
Basic

Failure (F)
Not even reaching marginal levels

Part III Other Information

Keyword Syllabus

Revision of Boolean algebra
Boolean algebra and switching functions; minterm and maxterm canonical forms; sum of products and products of sums; don’ t care conditions; minimization of Boolean algebra.

Combinational Logic Circuit Design
Minimization by Karnaugh map and Quine-McCluskey method; circuit designs; timing parameters and circuit hazards.

Circuit Design with Functional Blocks
Carry Look Ahead adder; comparators; decoders and encoders; multiplexers and demultiplexers.

Introduction to Hardware Description Language (HDL)
Introduction to Hardware Description Language (HDL); logic gates and combinational circuit modelling.

Flip-flops
Latches, RS, JK, D-type, edge-triggered and master-slave flip-flops; triggering and setting; timing parameters; HDL circuit modelling.

Synchronous Sequential Logic Circuit Design
Concept of states; Mealy and Moore Machines; redundant state elimination; sequential digital system analysis and design; HDL sequential circuit modelling.

Registers and Counter
Basic registers and counters; ripple counters and synchronous counters, and their applications; construction of registers and counters; HDL circuit modelling.

Field-Programmable Gate Array
Introduction to Look-up Table (LUT), Generic Array Logic (GAL), Programmable Array logic (PAL), simple programmable logic device, complex programmable logic device (CPLD), Field-Programmable Gate Array (FPGA), Programmable System-on-Chip (SoC).

FPGA Implementation
Combination and synchronous sequential circuit synthesis; datapath component description, debugging and validation.

Logic Families
Introduction to electrical characteristics of TTL and CMOS logic families; transfer characteristics, noise margins; fan-in and fan-out; comparison of families; interfacing between different families.

Reading List

Compulsory Readings

	Title
1	Nil

Additional Readings

	Title
1	Alan B. Marcovitz: Introduction to Logic Design, Third Edition, ISBN 978-0-07-016490-1 (McGraw-Hill Higher Education 2010).
2	Charles H Roth, Lizy K. John: Digital Systems Design Using VHDL, Fifth Edition, ISBN 978-1-305-63514-2 (Cengage Learning 2016).
3	C V S Rao: Switching Theory & Logic Design, ISBN 81-317-0183-2 (Pearson Education 2006).
4	Victor P. Nelson, H. Troy Nagle, Bill D. Carrol, J. David Irwin: Digital Logic Circuit Analysis and Design, ISBN 0-13-463894-8 (Prentice Hall, International Edition 1995).
5	William J. Dally: Digital design using VHDL: a systems approach, ISBN 978-1107098862, (Cambridge University Press, 2016).