Growth of pinhole-free ytterbium silicide film by solid-state reaction on Si(001) with a thin amorphous Si interlayer

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A thin amorphous Si (α-Si) interlayer is produced between the sputtering deposited ytterbium layer and Si(001) substrate, and the growth of the ytterbium silicide ($YbSi_{2-x}$) film is investigated in this paper. Formation of $YbSi_{2-x}$ was verified by x-ray diffraction (XRD). The silicide film morphology was examined by scanning electron microscopy (SEM) and atomic force microscopy (AFM). SEM results reveal that without the α-Si interlayer, pinholes form during $YbSi_{2-x}$ formation on Si(001). Furthermore, the XRD results demonstrate that there is a strong epitaxial relationship between the formed $YbSi_{2-x}$ and Si(001) substrate, and it is believed to be the reason for the formation of pinholes. To suppress the formation of pinholes, a thin α-Si interlayer with different thicknesses is introduced on the Si(001) substrate prior to Yb film deposition. The α-Si interlayer is produced by either sputter deposition employing a Si target or by Si ion implantation induced amorphization. In the presence of this thin α-Si interlayer, epitaxial growth of $YbSi_{2-x}$ is greatly suppressed even when the α-Si interlayer is so thin that full silicidation of the deposited Yb film still requires consumption of Si atoms from the Si(001) substrate. Fabrication of a pinhole-free $YbSi_{2-x}$ film is also demonstrated by SEM and AFM. The growth mechanism of the pinhole-free $YbSi_{2-x}$ film in the presence of a thin α-Si interlayer is discussed. © *2007 American Institute of Physics*.
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I. INTRODUCTION

Rare earth (RE) silicides are considered promising contact materials in nanometer scale *n*-channel metal-oxide-semiconductor field effect transistors (nMOSFETs) and *n*-channel Schottky barrier source/drain FET on account of their low Schottky barrier heights (SBHs) in contact with *n*-type Si.[1–4] Among the various types of RE silicides such as $ErSi_{2-x}$, $TbSi_{2-x}$, and $DySi_{2-x}$, $YbSi_{2-x}$ has recently been reported to have the most favorable characteristics from the perspective of low SBH applications.[5] However, in RE metal silicidation, Si is the dominant diffusion species and the Yb/Si(001) solid-state reaction is commonly plagued by pinhole formation.[6–11] Besides contamination induced pinhole formation mechanisms,[12–14] two other important pinhole formation models have been recently proposed. When a capping layer such as Mo or amorphous Si layer was employed, Luo and Chen proposed that the pinhole formation was related to the competition between the growth of the amorphous interlayer (mixed by RE metal and Si atoms) consisting of epitaxial RE silicide and that of the amorphous interlayer without epitaxial RE silicide.[15] The growth rate of the amorphous interlayer without epitaxial RE silicide is faster than that with epitaxial RE silicide, and so Si atoms diffusing from the substrate are nonuniform, thereby giving rise to the formation of recessed regions.[15] Eventually, the nonplanar nature of the $RESi_{2-x}$/Si(111) interface in the recessed regions leads to the formation of polycrystalline $RESi_{2-x}$ films on Si. Consequently, a large number of Si atoms from the Si substrate can diffuse laterally through the recessed regions that provide more rapid paths for atomic diffusion. Finally, the $RESi_{2-x}$ films inside the recessed regions break apart to form pinholes.[11,16,17] Travlos *et al.* have reported that in the absence of a capping layer, a continuous crystalline RE silicide interlayer forms during silicidation. However, the large compressive stress arising from volumetric changes of the reacted RE metal deforms the RE silicide layer, causing partial delamination and nonuniform Si diffusion from the substrate leading to pinhole formation.[18] According to these two models, nonuniform Si diffusion from the substrate is the common phenomenon causing pinhole formation. Techniques such as codeposition of RE metal and Si (Ref. 8) and employing an amorphous Si (α-Si) cap on RE metal[9,10] have been proposed to reduce pinholes. The crux of these methods is to minimize Si consumption, i.e., fewer Si atoms diffusing from the substrate, in order to retard pinhole formation.

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To suppress the formation of pinholes, in this paper a thin α-Si interlayer with different film thicknesses is introduced between the deposited Yb film and Si(001) substrate. With a Ti/TiN bicapping layer to suppress oxidation, our results indicate that introduction of the α-Si interlayer can effectively suppress the formation of pinholes and the production of a pinhole-free $YbSi_{2-x}$ film is demonstrated.

II. EXPERIMENTAL DETAILS

After a standard RCA clean and a final dip in diluted HF, p-type Si (001) wafers with resistivity of 4–8 Ω cm were immediately loaded into a Balzers physical vapor deposition (PVD) system with a base pressure lower than 2×10^{-5} Pa. Different film stacks including Ti(20 nm)/TiN(80 nm)/Yb(15 nm)/p-Si(001), Ti(20 nm)/TiN(80 nm)/Yb(15 nm)/α-Si(20 nm)/p-Si(001), and Ti(20 nm)/TiN(80 nm)/Yb(15 nm)/α-Si(10 nm)/p-Si(001) were prepared on the Si substrates at a pressure of 5×10^{-1} Pa by sputtering or reactive sputtering of high-purity Si, Yb, and Ti targets. After PVD, the samples were annealed *ex situ* in a lamp-based rapid thermal annealing (RTA) system at temperatures ranging from 400 to 800 °C with a soaking time of 60 s. The annealing ambient was high-purity N_2. After silicidation, the capping layers (Ti/TiN) and unreacted Yb were selectively wet etched in a mixture of sulfuric acid and hydrogen peroxide (H_2SO_4; H_2O_2=2:1) at 100 °C. X-ray diffraction (XRD) under Bragg-Brentano geometry was employed to identify the phases. Optical microscopy, scanning electron microscopy (SEM), and atomic force microscopy (AFM) were used to examine the surface morphology.

III. RESULTS

As shown in Fig. 1(a) after selective etching, $YbSi_{2-x}$ forms after annealing at 500 °C for 60 s on the samples without the α-Si interlayer. $YbSi_{2-x}$ has a hexagonal AlB_2 structure with lattice constants of $a=b=3.77$ Å and $c=4.10$ Å.[19] Also, it is well known that $YbSi_{2-x}$ films formed on Si(001) consist of two types of epitaxial grains with their (100) planes both parallel to Si(001) and their c axes 90° misorientated with each other [$YbSi_{2-x}(100)\|Si(001)$ and $YbSi_{2-x}\langle001\rangle\|Si(110)$ or $YbSi_{2-x}\langle001\rangle\|Si(1\bar{1}0)$]. The XRD results in Fig. 1(a) clearly show the strongly textured relationship between the $YbSi_{2-x}$ and Si(001) substrate as only very strong $YbSi_{2-x}(100)$ and (200) diffraction peaks are observed. Furthermore, consistent with Luo and Tsai's model,[11,15] pinholes appear in the $YbSi_{2-x}$ formed at 500 °C, as shown in Figs. 1(b) and 1(c). A similar surface morphology is revealed even after annealing at 700 °C, as shown in Fig. 1(d). A magnified AFM view of a typical defect detected in the sample annealed at 500 °C is shown in Fig. 1(e). The depth profiles of the defect shown in Figs. 1(f) and 1(g) demonstrate that its penetration depth (~50 nm) is several times of the silicide layer thickness (~18 nm). Thus, the defect is in the same type as reported by Chen's model.[10,11,15]

To break the epitaxial relationship, a 20 nm α-Si interlayer is deposited between the Yb film and Si(001) substrate. As shown in Figs. 2(a) and 2(b), $YbSi_{2-x}$ forms after 450 °C annealing and oxidation is effectively suppressed by Ti/TiN capping.[20] In contrast to the samples without the α-Si interlayer, pinholes disappear after 700 °C annealing, as shown in Fig. 2(c). The growth of pinhole-free $ErSi_{2-x}$ films on a 500 nm thick α-Si layer has also been reported before.[12] The XRD results in Fig. 2(b) disclose two additional peaks corresponding to $YbSi_{2-x}(101)$ and $YbSi_{2-x}(110)$. Moreover, the XRD results in Fig. 2(b) reveal that the $YbSi_{2-x}(100)$ peak intensity decreases significantly and its full width at half maximum (FWHM) becomes larger.

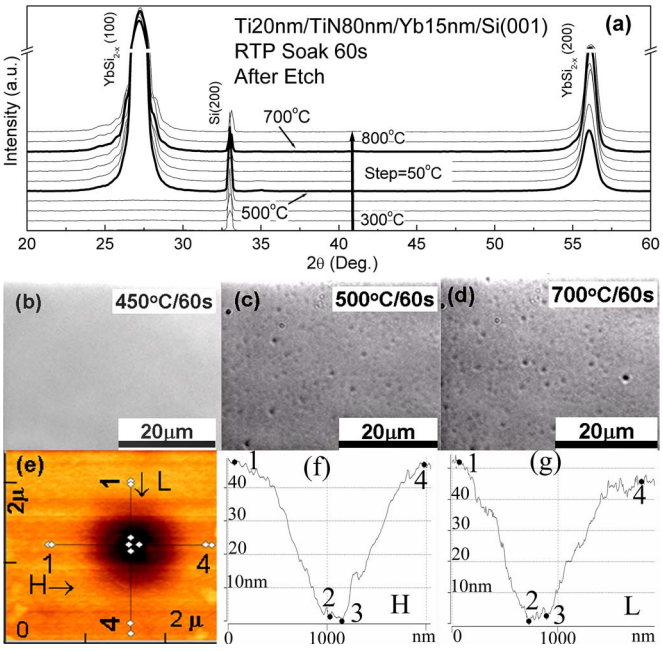

FIG. 1. (Color online) (a) XRD results for Ti(20 nm)/TiN(80 nm)/Yb(15 nm)/Si(001) samples annealed at various temperatures after selective etch. The optical microscopy pictures for Ti(20 nm)/TiN(80 nm)/Yb(15 nm)/Si(001) samples annealed at (b) 450 °C, (c) 500 °C, and (d) 700 °C after selective etch are also shown. (e) The surface morphology picture revealed by AFM for sample annealed at 500 °C shows the depth profiles of a typical pinhole defect, where the horizontal line (H) and longitude (L) line profiles are, respectively, plotted in (f) and (g).

During full silicidation, a 15 nm thick Yb film consumes about 15 nm of Si. Hence, no Si atoms from the Si(001) substrate are consumed during the silicidation reaction of the 15 nm thick Yb film in the presence of a 20 nm thick α-Si interlayer. To further investigate the influence of the α-Si interlayer on pinhole formation, a 10 nm thick α-Si interlayer is deposited between the Yb film and Si(001) substrate. In this case, full silicidation requires the consumption of Si atoms from the Si(001) substrate. As shown in Fig. 3(a), similar to the reaction on the 20 nm α-Si interlayer, $YbSi_{2-x}$ begins to form at 450 °C. Pinholes also completely disappear at 700 °C, as shown in the SEM picture in Fig. 3(b). The surface morphology of the sample annealed at 700 °C examined by AFM over a scanned area of 10×10 μm^2 is exhibited in Fig. 3(c). The root mean square surface roughness is as low as 0.78 nm, indicating a very smooth surface.

IV. DISCUSSIONS

Comparing the XRD results acquired from the samples with a 20 nm α-Si interlayer and 10 nm α-Si interlayer in Figs. 2(b) and 3(a), two common characteristics can be

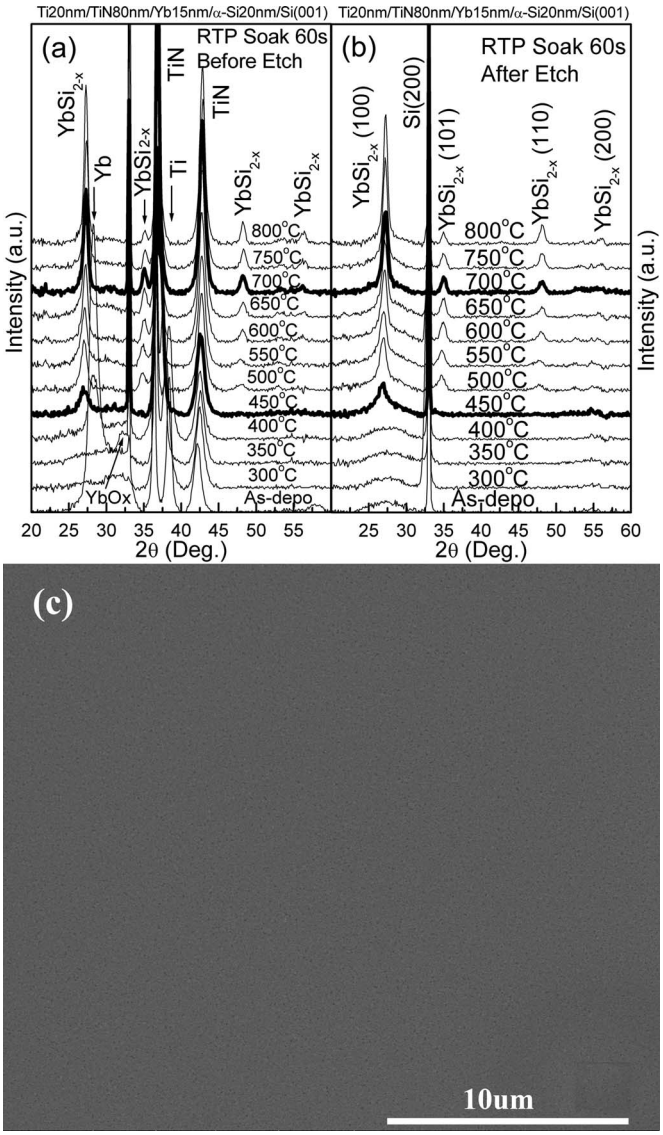

FIG. 2. XRD results for Ti(20 nm)/TiN(80 nm)/Yb(15 nm)/α-Si(20 nm)/Si(001) samples annealed at various temperatures (a) before selective etch and (b) after selective etch. (c) SEM picture for Ti(20 nm)/TiN(80 nm)/Yb(15 nm)/α-Si(20 nm)/Si(001) sample annealed at 700 °C after selective etch.

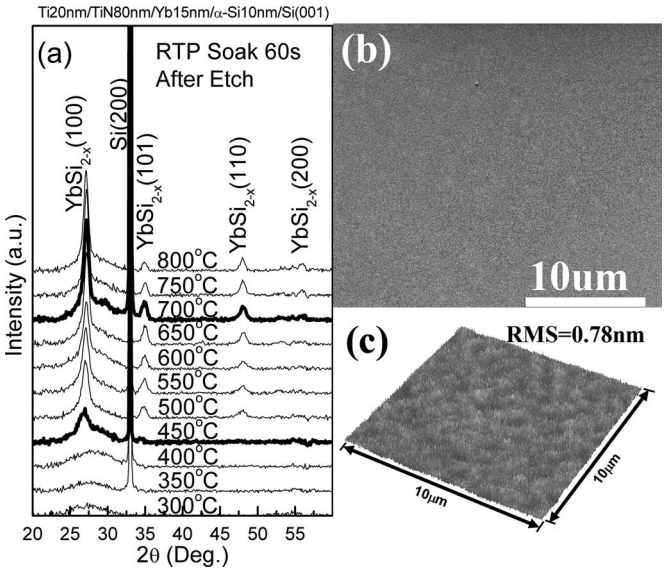

FIG. 3. (a) XRD results for Ti(20 nm)/TiN(80 nm)/Yb(15 nm)/α-Si(10 nm)/Si(001) samples annealed at various temperatures after selective etch. (b) SEM picture, and (c) AFM picture for Ti(20 nm)/TiN(80 nm)/Yb(15 nm)/α-Si(10 nm)/Si(001) sample annealed at 700 °C after selective etch.

found. Firstly, the $YbSi_{2-x}$ formation temperature is 50 °C lower than that on a single-crystalline Si(001) substrate as shown in Fig. 1(a), implying that the reaction barrier on α-Si is reduced. Secondly, the epitaxial relationship between the $YbSi_{2-x}$ and Si(001) is effectively suppressed, as indicated by the appearance of two more diffraction peaks of $YbSi_{2-x}$(101) and $YbSi_{2-x}$(110), larger FWHM of the main epitaxial peak of $YbSi_{2-x}$(100), as well as greatly decreased peak intensity, as shown in Fig. 4(a). The average $YbSi_{2-x}$ grain size can be estimated by the following formula:[21]

$$L = \frac{k\lambda}{\beta \cos \theta}, \tag{1}$$

where $k \approx 0.9$, λ is the incident x-ray wavelength, β is the FWHM of the diffraction peak, and θ is the diffraction angle. In principle, β should be obtained after subtracting the instrumental broadening width from the original FWHM. For small grains, the correction ought to be insignificant. Consequently, the average grain sizes L in the samples without the α-Si interlayer and those with 10 and 20 nm thick α-Si interlayer are about 17.6, 12.7, and 12.3 nm, respectively. Because a 15 nm thick Yb will finally form about 18 nm of $YbSi_2$, the average grain size of 17.6 nm in the sample without the α-Si interlayer indicates that the $YbSi_{2-x}$ grains grow almost epitaxially throughout the silicide layer. In comparison, the average grain size for silicidation with 20 and 10 nm α-Si interlayer, is much smaller than that in the sample without the α-Si interlayer, and it is also smaller than the entire silicide layer thickness (~18 nm). This indicates that more than one $YbSi_{2-x}$ grain layer is stacked together in the formed silicide film and so the film is more polycrystalline.

The single-crystalline Si(001) substrate provides the epitaxial template for $YbSi_{2-x}$ formation. If the epitaxial relationship between the nucleated $YbSi_{2-x}$ islands and Si(001) substrate is disrupted, not only does the $YbSi_{2-x}$ grain size become smaller but also uniform Si diffusion from the substrate may occur. Therefore, a pinhole-free $YbSi_{2-x}$ layer may form. Actually, when an α-Si interlayer is used, due to the break of the epitaxial template, a uniform, thin $YbSi_{2-x}$ layer can form in the early stage during annealing.[18] As the reaction continues, Si atoms being the dominant diffusion species continue to diffuse from the underlying α-Si layer via the thin $YbSi_{2-x}$ layer to the Yb/$YbSi_{2-x}$ interface and react with Yb. The $YbSi_{2-x}$ grain size in the sample with the α-Si interlayer is smaller than that on single-crystalline Si, as shown in Fig. 4(a), and therefore, there are more grain boundaries for the Si atoms to diffuse uniformly through the $YbSi_{2-x}$ layer. Moreover, the amount of epitaxial $YbSi_{2-x}$ grains in the sample with an α-Si interlayer is significantly reduced as revealed by the greatly decreased $YbSi_{2-x}$(100) diffraction peak intensity in Fig. 4(a). It is believed that Si diffusion through the grain boundaries between two ran-

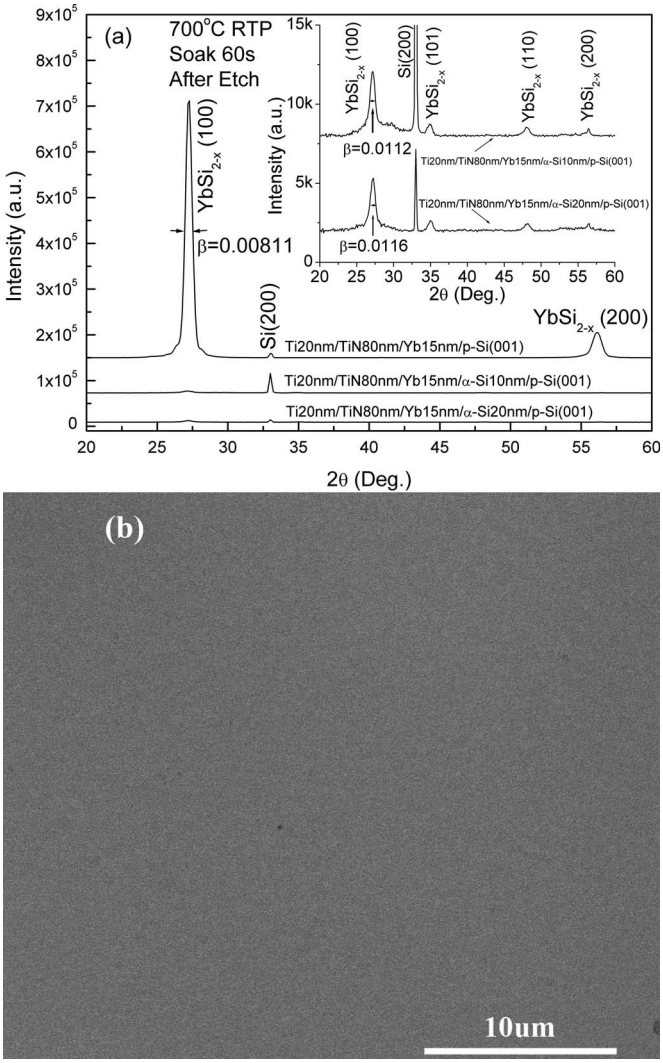

FIG. 4. (a) XRD results for Ti(20 nm)/TiN(80 nm)/Yb(15 nm)/Si(001), Ti(20 nm)/TiN(80 nm)/Yb(15 nm)/α-Si(10 nm)/Si(001), and Ti(20 nm)/TiN(80 nm)/Yb(15 nm)/α-Si(20 nm)/Si(001) samples annealed at 700 °C after selective etch. With a more suitable Y scale, the inset shows the same XRD results for the samples with α-Si(10 nm) and α-Si(20 nm). β represents the FWHM of the diffraction peak. (b) SEM picture for Ti(20 nm)/TiN(80 nm)/Yb(15 nm)/α-Si(10 nm)/Si(001) sample annealed at 700 °C after selective etch. The α-Si layer was realized by Si ion implantation at 1 keV with a dose of $3\times15/\mathrm{cm}^2$.

domly orientated grains is much easier than that through those grain boundaries between two adjacent epitaxial grains. In this growth model, fast lateral diffusion of Si atoms resulting in pinhole formation[16,17] is suppressed, and a smooth $YbSi_{2-x}/\alpha$-Si interface will remain until the α-Si layer is depleted, for example, in the reaction between the 15 nm thick Yb and underlying 10 nm thick α-Si interlayer. However, when the α-Si layer is totally consumed, a polycrystalline $YbSi_{2-x}$ layer with random grain orientations forms. A higher activation energy is required for the epitaxial reaction of these grains on Si(001) by readjusting the orientations and thus the epitaxial growth of $YbSi_{2-x}$ is suppressed. Moreover, with more grain boundaries due to the smaller $YbSi_{2-x}$ grain size, it is believed that Si diffusion through the grain boundaries between two randomly orientated grains is also easier. Therefore, even after the α-Si layer has been completely consumed, the uniform Si atom diffusion out of the Si(001) substrate can still be realized, and then a pinhole-free $YbSi_{2-x}$ film may form. In fact, with a 5 nm thick α-Si interlayer for the silicidation of 15 nm Yb, a uniform silicide layer is also observed in our experiments. Besides the PVD-deposited α-Si interlayer, Si ion implantation is also performed into some substrates to obtain a thin (~10 nm) amorphous Si surface layer on the Axcelis GSD 300 implanter at 1 keV with a Si dose of $3\times15/\mathrm{cm}^2$. This process is more compatible with standard semiconductor processing and, similarly, pinhole-free $YbSi_{2-x}$ silicide layer can be obtained, as shown in Fig. 4(b).

V. CONCLUSION

In summary, a thin α-Si interlayer is introduced between the sputtering deposited Yb layer and the Si(001) substrate, and the growth of $YbSi_{2-x}$ film by solid-state reaction is investigated in this paper. The results reveal that the α-Si interlayer can effectively suppress the epitaxial growth of $YbSi_{2-x}$ on Si(001). It is also demonstrated that a pinhole-free $YbSi_{2-x}$ layer can be fabricated by introducing such a thin α-Si interlayer even if the α-Si interlayer is so thin that full silicidation of the deposited Yb film still requires the consumption of Si atoms from the Si(001) substrate.

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