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Recent Advances and Applications of Plasma Immersion Ion Implantation

Paul K Chu*
Department of Physics & Materials Science, City University of Hong Kong, Kowloon, Hong Kong, China
*Email: paul.chu@cityu.edu.hk

Abstract

Many new applications of plasma immersion ion implantation (PIII) have recently emerged. In addition to the surface modification and fabrication of conventional metallurgical and semiconductor materials and structures by PIII, new areas such as biomedical materials engineering and plasma treatment of insulating materials have attracted much attention. In this paper, the progress of our recent research work of PIII on microelectronics, namely optical characteristics of hydrogen plasma implanted silicon and fabrication of novel silicon-on-insulator materials, are described.

1. Introduction

Low temperature photoluminescence in the infrared region of hydrogen implanted single crystalline silicon have been investigated. The beam-line ion implanted samples show a broad photoluminescence band below the band gap, whereas the PIII implanted samples show at least one more peak at 1.17eV and a much wider photoluminescence band. The origins are investigated and the peak at 1.17 eV appears to originate from non-phonon emission enhanced by lattice disorder. Our results suggest that PIII may be a better technique than beam-line ion implantation in introducing a certain disorder into the silicon lattice to circumvent the conservation of quasi-momentum and consequently enhance the light emission efficiency from the modified Si samples. We have also conducted work to replace the buried SiO_2 layer in silicon-on-insulator (SOI) with a plasma synthesized diamond-like-carbon (DLC) thin film to mitigate the self-heating effects. The DLC films synthesized on silicon by a special plasma immersion ion implantation & deposition (PIII&D) process exhibit outstanding surface topography, and excellent insulated properties are maintained up to an annealing temperature of 900°C. Hence, the degree of graphitization in our DLC materials is insignificant during thin-film transistor (TFT) processing and even in most annealing steps in conventional CMOS (Complementary metal oxide silicon) processing. Using Si/DLC direct bonding and the hydrogen-induced layer transfer method, a silicon-on-diamond (SOD) structure has been successfully fabricated. Cross-sectional high-resolution transmission electron microscopy reveals that the bonded interface is abrupt and the top Si layer exhibits nearly perfect single crystalline quality. A model is postulated to describe the reactions occurring at the interface during the annealing steps in Si-DLC wafer bonding.

2. Optical Properties of Hydrogen Plasma Implanted Silicon

Silicon-based luminescence [1] is of great interest due to possible integration of optoelectronics into the mature silicon integrated circuit technology. Much work has been conducted to investigate low dimensional structures such as porous Si [2], and Si nanodots embedded in SiO_2 [3] or introducing new luminescence centers into Si materials [4]. In contrast, there have been fewer reports on lattice disordering of Si materials to alter the light emission efficiency. It has been proposed that disorder-induced weak confinement can widen the bandgap and also turn the bandgap into a direct-like one due to relaxation of momentum conservation caused by disorder [5]. However, no further reports have been be published possibly due to the difficulty in realizing the exact microstructure of the proposed disorder in the Si lattice.

Hydrogen - implanted silicon has recently attracted much interest [6] in the ion-cut technology for silicon-on-insulator (SOI) fabrication [7]. In this method, a large dose of hydrogen is implanted into silicon to create a buried layer consisting of micro-cavities or bubbles to facilitate layer transfer. This hydrogen - implanted region also exhibits interesting optical characteristics and is more stable than traditional porous silicon (PS) produced by anodic etching. However, the luminescence mechanism in this material is not understood and most of the previous experiments [8, 9] have focused on the luminescent lines and broad bands below the band gap of silicon. An extremely weak band at about 0.78 μm (visible region) has been reported [10], but its origin is still unclear.

Therefore, there is interest in exploring the optical properties of hydrogen implanted silicon. In this work, H_2^+ ions were implanted at 25kV and the doses were 4×10^{15} cm^{-2} and 2×10^{16} cm^{-2} for the two different groups of samples. Four different sample voltages: -10kV, -15kV, -20 kV and -25kV were used to produce four sets

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of samples. The pulse duration and repetition rate in the PIII experiments were 30 μs and 200 Hz, respectively. The dose was estimated to be about 10^{16} cm^{-2} based on the current waveform.

Fig. 1 exhibits a typical PL spectrum from the beam-line implanted samples as a function of annealing temperature, measured at 11 K with a 514.5 nm argon laser. For the as-implanted sample, a weak PL band below the silicon band gap peaking at ~1.4 μm is observed. No significant changes can be detected after annealing at 200°C for 30 minutes, but annealing at 400°C results in a blue shift and a new, stronger luminescence peak at a higher energy appears. However, after annealing at 600°C, the entire luminescence band vanishes. This dependence with annealing temperature is quite similar to those of peaks at ~0.78μm, ~1.25μm and ~1.5μm reported previously [10]. Large dose H implantation into Si creates many kinds of defects, platelets and also Si-H and/or Si-OH complexes, all of which possibly contribute to the final PL band. During annealing, H interacts with these features and thus modulates the PL band. With increasing temperature (T), hydrogen becomes more mobile and decorates some point defects. Passivation of the dangling bonds prevents non-radiative recombination at these centers resulting in an increase of PL intensity. At T>500°C, H out-diffuses and the dangling bonds become non-radiative recombination centers again. Therefore, the PL band vanishes in the 600°C sample. The PL band observed in our experiments includes two bands at ~1.25μm and ~1.5μm assigned to the recombination of carriers at hydrogen stabilized platelet defects or recombination of carriers localized by the strain field in the damaged regions.

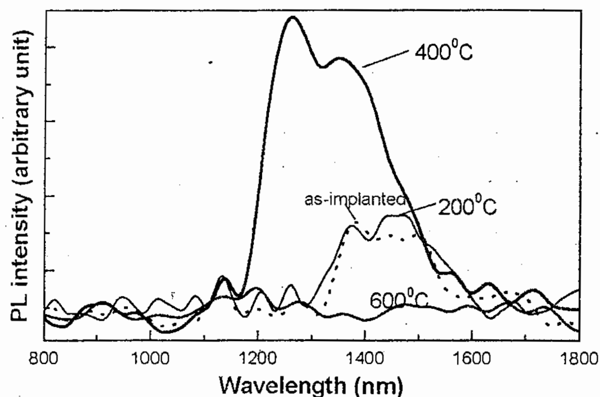

Figure 1. PL spectrum versus annealing temperature from beam-line implanted sample (25 kV, 2x10^{16} cm^{-2} with H_2^+ ions) measured at 11K with an argon laser excitation source (λ = 514.5 nm, power = 400mW).

Our results show that the 400°C sample exhibits the strongest PL intensity. Fig. 2 depicts the results also measured at 11 K for all the samples annealed at 400°C. For comparison, the PL result from an un-implanted silicon sample is also given as a dotted line. The spectrum shows two narrow PL bands/lines located at ~1134 nm (strong) and 1200 nm (weak). They are due to the boron-bound-exciton [B(BE)] recombination. The dominant emission at ~1134 nm comes from momentum-conserving transverse optical (B_{TO}) phonon replicas of the B(BE) at 1.093eV (1134nm). The one at 1200nm may originate from several phonon replicas such as B_{TO} + O^{Γ} (O^{Γ} is the zone-center optical phonon) at 1.021eV and the two-hole transition leaving the acceptor hole in an excited state after recombination, B_{TO} + B^*_h at 1.050eV. After hydrogen implantation and annealing at 400°C for 30 minutes, all samples exhibit a broad PL band near the band gap. The original peaks at 1134 nm and 1200 nm cannot ~~be distinguished~~ clearly because the surface layer has been damaged by ion implantation and the PL signal mainly comes from this surface layer.

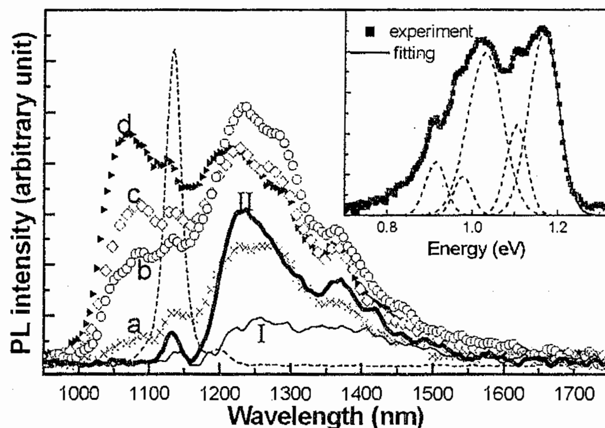

Figure 2. PL spectrum acquired at 11K from the 400°C annealed samples. (I): beam-line, 25 kV, 2x10^{16} cm^{-2}; (II): beam-line, 25 kV, 4x10^{15} cm^{-2}; (a): PIII, -10kV; (b): PIII, -15kV; (c): PIII, -20kV and (d): PIII, -25kV. The dotted line depicts the single crystal Si band edge emission, as a reference line. The inset gives a Guassian fitting for sample (d). Five peaks are used but the actual peak may have more than 5 components.

It is obvious that for the beam-line implanted samples, only emission below the band gap can be observed, while emission both below and above (very near) the band gap can be observed from the PIII and annealed samples. In Fig. 2, for beam-line implantation, the lower dose (4x10^{15} cm^{-2}) sample shows stronger intensity than the higher dose one. It is thus believed that a lower dose creates a smaller number of defects such as

dangling bonds resulting in a smaller number of non-radiative recombination centers. For the PIII samples, in addition to the peaks observed for the beam-line samples, at least one more PL peak at higher energy (1.17 eV) that is approximately equal to the band gap (1.166 eV at 0K) of Si can be observed. From the viewpoint of bandgap evolution, our results provide direct evidence of bandgap widening after PIII. The intensity of this peak increases with increasing bias voltage, whereas the intensity of the peaks below the band gap does not exhibit an obvious monotonic dependence on the bias. In addition, the PL results acquired at different temperatures (not shown here) indicate that all the features in the PL band decrease with increasing measurement temperature.

In order to elucidate the mechanisms of the PL results, the deconvoluted PL band into several (≥5) peaks as shown in the inset of Fig. 2 suggesting that no less than five components contribute to the final PL spectrum. At present, we are not able to exactly assign the origin of each component. Below the band gap, it is believed that the peak at ~1360 nm (~0.91 eV) comes from the hydrogen stabilized {111} platelet. It is believed that the other two peaks below the band gap are due to recombination of carriers at hydrogen stabilized platelet defects or carriers localized by the strain field , as mentioned above. The peak at ~1.1 eV originates from phonon replicas of B(BE) in our samples.

For the peak at 1.17 eV, we analyze its origin according to the difference between beam-line implantation and PIII. Since voltage pulses are applied in PIII, there are many low energy ions during the rise time and fall time of each sample pulse and they cause substantial damage and even amorphization. In our XTEM micrograph (not shown here), the surface layer is greatly damaged during implantation as indicated by the electron diffraction pattern. It has two possible effects. Firstly, the band gap is enlarged since the band gap of a-Si (1.6eV) is higher than that of crystalline Si (1.1eV). Secondly, momentum conservation is no longer necessary due to the disordered lattice, resulting in enhanced efficiency of non-phonon emission. Thus, we attribute the peak at 1.17eV to non-phonon emission in the heavily damaged surface layer. This agrees well with the fact that a higher bias voltage results in a thicker surface damaged layer. In fact, according to high resolution transmission electron microscopy results, the PIII damaged layer is different from an amorphous microstructure that is completely disordered. Although PIII destroys the original long-distance order in the crystal lattice, the final structure retains a certain order or short-distance order and thus can be considered as a medium state between single crystal (long-distance order) and amorphous structure (disorder). This unique microstructure, which agrees well with the so-called "quantum sieves", produces Anderson localization and hence weak confinement. Consequently the non-phonon emission at about 1.17eV is greatly enhanced.

Elicited by the results described above, we made some porous Si (PS) samples using traditional anodic etching method and then performed plasma implantation at −10kV at a base pressure of 4.6×10^{-6} Torr and a working pressure of 5.8×10^{-4} Torr. As expected, the PL results acquired at room temperature with a He-Cd laser source (325nm) confirm that the PL band at 550~850 nm is greatly increased by plasma implantation, whereas the weak band at about 420 nm remains almost unchanged. It is reasonable since the PL band at ~420nm comes from O-related complexes and the strong PL peak at 550~850nm originates from nano-size Si in PS. This proves that the emission efficiency in these nano-size Si structures is improved by implantation and thus corroborates the conclusion drawn from hydrogen-implanted silicon.

3. Synthesis of Silicon-on-Diamond by Plasma Immersion Ion Implantation

Silicon-on-insulator (SOI) MOSFET is expected to replace conventional bulk silicon substrates in many microelectronic devices because it possesses many advantages such as the reduction of parasitic capacitance, excellent sub-threshold slope, elimination of latch up, and resistance to radiation [11]. However, wider applications of SOI in ULSI are hampered by the self-heating effects caused by the poor thermal conductivity of the buried silicon dioxide layer [12]. Hence, it is important to explore alternative buried insulators with better thermal conductivity.

The ion-cutting technique that involves hydrogen-induced wafer cleavage and wafer bonding has become one of the major SOI fabrication techniques [13]. Using this technology, an insulator possessing higher thermal conductivity can substitute for the buried silicon dioxide. One of the interesting buried insulators is crystalline diamond with a thermal conductivity about 1000 times higher than that of SiO_2 (~2000W/m·K versus 1.4W/m·K). However, its rough surface prohibits direct bonding to silicon wafers without extensive polishing and surface treatment. In comparison, a diamond-like-carbon (DLC) thin film possesses thermal properties similar to those of crystalline diamond while retaining high electrical resistivity. Due to this unique combination of properties, a DLC buried layer can in principle

outperform the buried silicon dioxide layer in SOI. Yushin et al. [14] investigated the application of diamond to SOI technology. However, mechanical polishing was necessary in order to reduce the surface roughness of the polycrystalline diamond film before direct bonding. Song et al. [15] proposed the use of tetrahedral amorphous carbon thin films in SOI, but they only reported the properties of the carbon films without fabricating a real silicon-on-carbon structure. In this letter, we report the successful formation of a silicon-on-DLC (SOD) structure using ion cutting and Si / DLC direct bonding.

The DLC thin films were fabricated on 100mm *p*-type Si (100) wafers using plasma immersion ion implantation & deposition (PIII&D) [16]. The details of this PIII-D system have been reported elsewhere [17, 18]. During deposition, a mixture of acetylene (20 sccm) and argon (5sccm) was bled into the chamber to a working pressure of 8×10^{-4} Torr, and the plasma was sustained by a 500W radio frequency (RF) source. The applied voltage, repetition rate, and pulse width were –20kV, 40Hz and 400μs, respectively. The deposition time was 120 minutes. These experimental conditions were selected based on many trial experiments in order to produce the smoothest surface while maintaining high electrical resistivity. After deposition, one set of samples were furnace annealed at 500 to 1000 °C in a N_2 ambient for 1 hour. The other samples underwent rapid thermal annealing (RTA) at 900°C and 1000°C for 30 seconds also in a N_2 ambient.

To fabricate the SOD structure, the DLC-coated acceptor wafer was bonded to a Si donor wafer that had been implanted with 6×10^{16} cm^{-2} hydrogen at 60 kV. Before direct bonding, both the acceptor and donor wafers were cleaned with a H_2SO_4: H_2O_2 (10:1) solvent at 120°C for 10 mins, followed by rinsing in de-ionized (DI) water and spin drying. The surfaces were then activated in a 400W oxygen plasma (oxygen pressure of 1.3 Torr) at 100°C for 60 seconds. After activation, they were dipped in a modified RCA-1 solution (NH_4OH: H_2O_2: H_2O = 1: 6: 30) at 70-75°C for 60 seconds, followed by rinsing in DI water and spin drying again. Afterwards, the two wafers were placed with the mirror surfaces facing each other separated by three removable spacers in air at room temperature. Direct bonding occurred over the entire surface of the wafers within seconds under a small applied pressure at the center by tweezers after removing the spacers. After bonding, the pair was heated to 120°C for 2 hrs in air, and the temperature was raised to 200°C for another 10 hrs to improve the bonding strength. Subsequently, the bonded wafer was furnace annealed at 300°C for 2 hrs under nitrogen and the temperature was finally raised to 450°C for 10-15 mins to induce splitting of the thin Si layer to complete the transfer of a thin silicon layer onto the DLC-coated silicon wafer.

In the ion-cutting process, whether or not direct bonding is successful or not depends very much on the surface morphology of the DLC film. Therefore, AFM was performed initially to examine the surface topography of our as-deposited DLC film. Using our special experimental protocols, the surface of the DLC film is very smooth and uniform with a surface roughness RMS value of 0.381 nm that is good enough for direct bonding obviating the needs for complicated lapping and polishing procedures. It should be emphasized that the excellent surface topography is a direct result of our special PIII&D process. The optimal ion energy creates good film adhesion as well as excellent surface flatness, both of which not easily accomplished using conventional low-energy CVD deposition techniques.

In addition to the surface morphology, a high electrical resistivity is crucial to the successful operation of devices fabricated in the SOI structure. It is common knowledge that graphitization of DLC can decrease the electrical resistivity significantly. In order to investigate the graphitization trend in our DLC films during high temperature annealing, we determined the breakdown electric fields of the as-deposited and annealed samples. The breakdown field that reflects the insulating property of the thin film can be determined by the current-voltage (*I-V*) characteristic measured from a metal/DLC/Si MIS structure. Fig. 3 shows the electrical breakdown fields of the samples as a function of annealing temperature. The breakdown field of the as-deposited DLC film is 4.2 MV/cm which compares reasonably well with previously reported results [15]. When the samples were annealed in the furnace at temperatures under 900°C, the breakdown fields did not change. When the anneal temperature reached 900 °C, the breakdown field began to decrease, but the changes were not obvious. However, when the temperature was increased to 1000°C, the breakdown field diminished significantly. It can be inferred that graphitization of our materials does not become significant until the annealing temperature reaches 1000°C and our Raman results (not shown here) are consistent with the electrical measurements. The RTA results (open circles in Fig. 3) indicate that after RTA at 900°C or 1000°C, no appreciable graphitization can be detected from our electrical data. Based on our results, the DLC synthesized using the special PIII&D process can

withstand furnace annealing and RTA up to 900°C, making it compatible with TFT and even conventional CMOS processing.

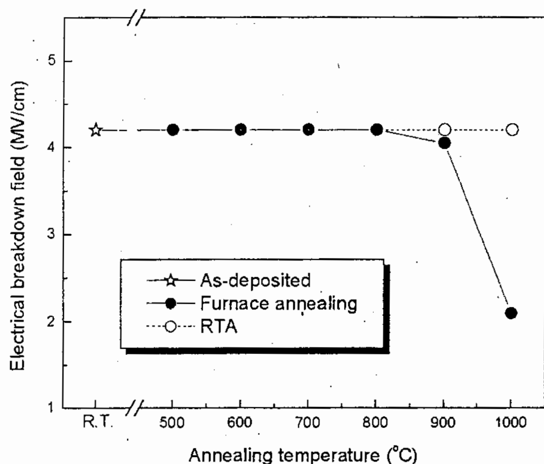

Figure 3. Influence of the annealing temperature on the electrical breakdown fields for the DLC films. Filled and open circles, respectively, represent results from furnace annealing and RTA in nitrogen ambient. The star is the result from the as-deposited sample.

In order to exam the quality of the bonding interface of the SOD structure, transmission electron microscopy (TEM) was employed. Fig. 4(a) depicts the micrograph of the bonded structure showing direct evidence of the formation of the SOD structure. The thicknesses of top Si layer and buried DLC layer are about 550~600 nm and 100 nm, respectively. The damaged surface region can be easily etched away and the top silicon layer can be further reduced to the desirable thickness by dry etching. Fig. 4(b) displays the high-resolution TEM image of the interfacial region between the top Si layer and buried DLC layer. The DLC layer is homogeneous and amorphous, while the Si atoms are well aligned without showing any observable structural defects. It is evident that single crystalline Si extends to the Si-DLC boundary, and the interface is as sharp as a few atomic layers. Our results clearly indicate that our process is capable of producing nearly perfect single crystal Si on DLC.

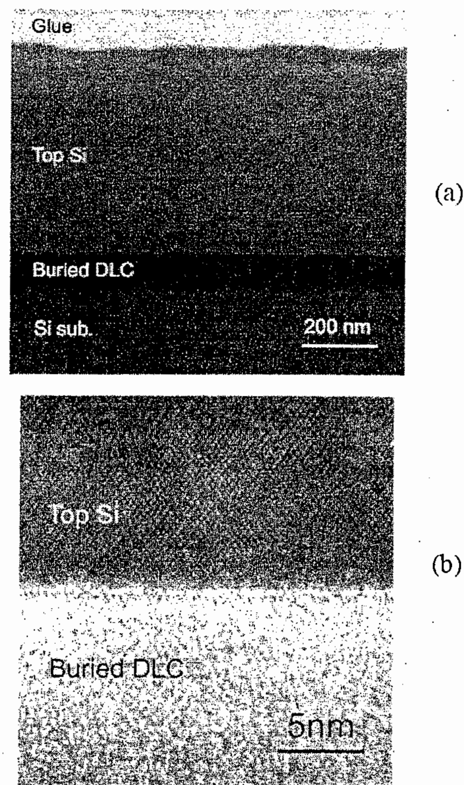

Figure 4. (a) TEM micrograph of the SOD structure formed using direct wafer bonding and hydrogen-induced layer transfer. (b) HRTEM micrograph of the interfacial region between the top Si layer and buried DLC layer, indicating a defect-free and single crystal Si layer and abrupt bonded interface.

4. Conclusion

In summary, we have successfully produced high-quality and heat-resistant silicon-on-diamond materials. The DLC films synthesized by our special PIII&D process exhibit outstanding surface topography and maintain excellent insulating characteristics up to an annealing temperature of 900°C. This bodes well for TFT as well as CMOS processing. The bonded interface is sharp and the top Si layer has almost perfect crystal quality. A simple model is proposed to describe the reactions occurring at the interface during the heating steps in the Si-DLC bonding process.

Acknowledgments

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