# CHAPTER 7: Polysilicon and Dielectric Film Deposition

Films of various materials are used in VLSI. In addition to being parts of the active devices, deposited thin films provide conducting regions within a device, electrical insulation between metals, and protection from the environment. The most widely used thin films in microelectronics are: (1) polycrystalline silicon or polysilicon, (2) doped or undoped silicon dioxide, and (3) stoichiometric or plasma-deposited silicon nitride. Metal film deposition will be covered in Chapter 10.

Polysilicon serves as:

(1) Gate electrode material in MOS devices

(2) Conducting materials for multilevel metallization

(3) Contact materials for devices with shallow junctions.

Polysilicon can be undoped or doped with elements such as As, P, or B to reduce the resistivity. The dopant can be incorporated in-situ during deposition, or later by diffusion or ion implantation. Polysilicon consisting of several percent oxygen is a semi-insulating material for circuit passivation.

Dielectric materials are used for:

(1) Insulation between conducting layers

(2) Diffusion and ion implantation masks

(3) Diffusion sources (doped oxide)

(4) Capping doped films to prevent dopant loss

(5) Gettering impurities

(6) Passivation to protect devices from impurities, moisture, and scratches

Phosphorus-doped silicon dioxide, commonly referred to as P-glass or phosphosilicate glass (PSG), is especially useful as a passivation layer because it inhibits the diffusion of impurities (such as Na), and it softens and flows at 950$^{o}$C to 1100$^{o}$C to create a smooth topography that is beneficial for depositing metals.

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Borophosphosilicate glass (BPSG), formed by incorporating both boron and phosphorus into the glass, flows at even lower temperatures between 850$^{o}$C and 950$^{o}$C. The smaller phosphorus content in BPSG reduces the severity of aluminum corrosion in the presence of moisture.

Silicon nitride is a barrier to sodium diffusion, is nearly impervious to moisture, and has a low oxidation rate. The local oxidation of silicon (LOCOS) process also uses silicon nitride as a mask. The patterned silicon nitride will prevent the underlying silicon from oxidation but leave the exposed silicon to be oxidized. Silicon nitride is also used as the dielectric for DRAM MOS capacitors when it combines with silicon dioxide.

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## 7.1 Physical Vapor Deposition (PVD)

Physical vapor deposition (PVD) technologies fall into two typical classes. Evaporation is one of the oldest techniques for depositing thin films. A vapor is first generated by evaporating a source material in a vacuum chamber and then transported from the source to the substrate and condensed to a solid film on the substrate surface.

Sputtering involves the ejection of surface atoms from an electrode surface by momentum transfer from the bombarding ions to the electrode surface atoms. The generated vapor of electrode material is then deposited on the substrate. Sputtering processes, unlike evaporation, are very well controlled and generally applicable to all materials such as metals, insulators, semiconductors, and alloys. A schematic diagram of a sputtering system is displayed in ***Figure 7.1***.

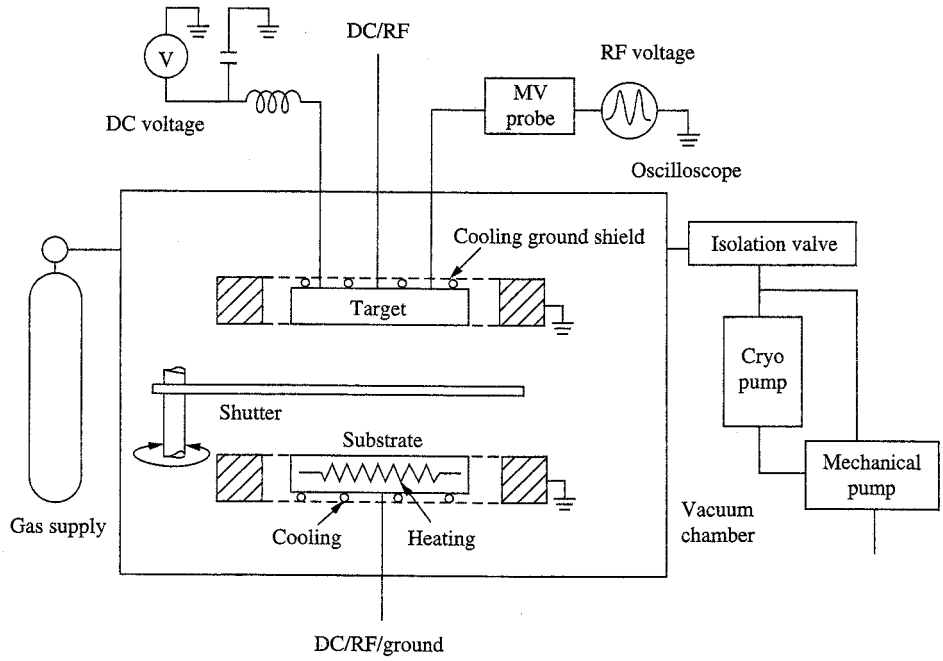


***Figure 7.1***: Diagram of a typical sputtering system.

## 7.2 Chemical Vapor Deposition (CVD)

The common CVD methods are: (1) atmospheric-pressure chemical vapor deposition (APCVD), (2) low-pressure chemical vapor deposition (LPCVD), and (3) plasma-enhanced chemical vapor deposition (PECVD). A comparison between APCVD and LPCVD shows that the benefits of the low-pressure deposition processes are uniform step coverage, precise control of composition and structure, low-temperature processing, high enough deposition rates and throughput, and low processing costs. Furthermore, no carrier gases are required in LPCVD reducing particle contamination. The most serious disadvantage of LPCVD and APCVD is that their operating temperature is high, and PECVD is an appropriate method to solve this problem. ***Table 7.1*** compares the characteristics and applications of the three CVD processes.

***Table 7.1***: Characteristics and applications of CVD processes.

| Process | Advantages | Disadvantages | Applications |
|---|---|---|---|
| APCVD (low T) | Simple reactor, fast deposition, low temperature | Poor step coverage, particle contamination, low throughput | Doped/undoped low T oxides |
| LPCVD | Excellent purity & uniformity, conformal step coverage, large wafer capacity, high throughput | High temperature, low deposition rate | Doped/undoped high T oxides, silicon nitride, polysilicon, tungsten, $WSi_2$ |
| PECVD | Low temperature, fast deposition, good step coverage | Chemical (e.g. $H_2$) and particle contamination | Passivation (nitride), low T insulators over metals |

***Fig. 7.2*** depicts the sequence of reaction steps in a CVD reaction. Because the deposition process includes force convection, boundary-layer diffusion, surface absorption, decomposition, surface diffusion, and incorporation, there are several

variables to be controlled. Temperature, pressure, flow rate, position, and reactant ratio are important factors for high-quality films.

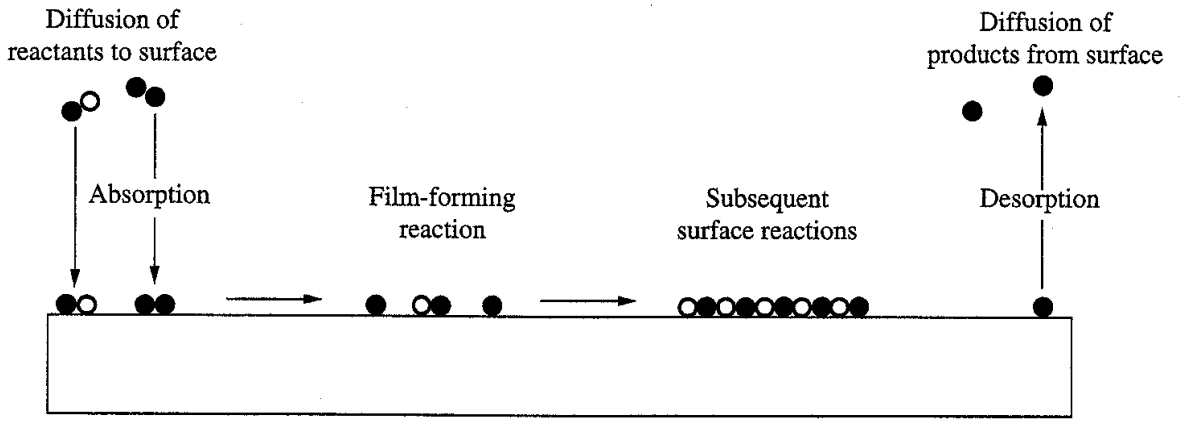


***Figure 7.2***: Sequence of reaction steps in a CVD process.

Since the steps in a CVD process are sequential, the one that occurs at the slowest rate will determine the deposition rate and the rate-determining steps can be grouped into gas-phase and surface processes. Gas-phase processes dictate the rate at which gases impinge on the surface and since such transport processes occur by gas-phase diffusion proportional to the diffusivity of the gas and the concentration gradient across the boundary layer, they are only weakly influenced by the deposition temperature. On the other hand, the surface reaction rate is greatly affected by the deposition temperature. At low temperature, the surface reaction rate is reduced so much that the arrival rate of reactants can exceed the rate at which they are consumed by the surface reaction process. Under such conditions, the deposition rate is surface-reaction-rate-limited, and at high temperature, it is usually mass-transport-limited. ***Figure 7.3*** illustrates that the deposition rate of a polysilicon CVD process increases rapidly with temperature. The temperature dependence is exponential and follows the Arrhenius equation:

$$R = A \exp\{-qE_a / kT\} \qquad \textit{(Equation 7.1)}$$

where $R$ is the deposition rate, $A$ is the frequency factor, $q$ is the electronic charge, $E_a$ is the activation energy, $k$ is the Boltzmann's constant, and $T$ is the absolute temperature. The activation energy calculated from the slope of the straight-line plots is roughly 1.7 eV. Although *Equation 7.1* predicts that the deposition rate increases with temperature, it is not so at high temperatures

because the reaction becomes faster than the rate at which unreacted silane arrives at the surface. The reaction in this temperature regime is mass-transport limited, as exemplified by the high temperature (or small 1/*T*) data depicted in ***Figure 7.3***. The linear portion of the lines in ***Figure 7.3*** show the surface-reaction limited conditions, that is, the rate of reaction is slower than the rate of reactant arrival.

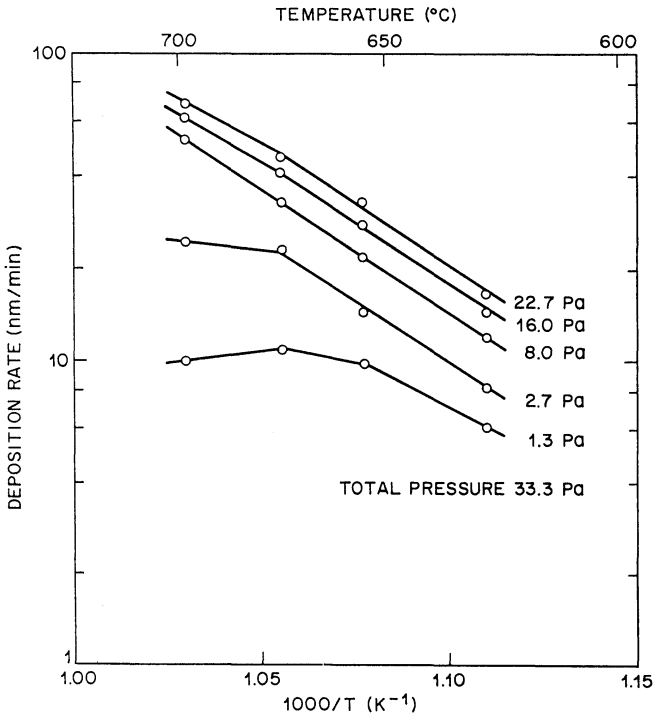


***Figure 7.3***: Arrhenius plot for polysilicon deposition for different silane partial pressures.

A CVD method is categorized not only by the pressure regime but also by its energy input. PECVD can employ a radio frequency (RF) power to generate glow discharge to transfer the energy into the reactant gases, allowing deposition at reduced temperature. In addition to this low deposition temperature advantage, other desirable attributes include good adhesion, low pinhole density, good step coverage, adequate electrical properties, and compatibility with pattern transfer processes.

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## ***Example 7.1***

If LPCVD polysilicon deposition has an activation energy of 1.65 eV and a deposition rate of 8 nm/min at 600°C, what is the deposition rate at 620°C?

**Solution**

Using the Arrhenius equation gives

$$R_1 = R_o e^{-\frac{qE_a}{kT_1}} \text{ and } R_2 = R_o e^{-\frac{qE_a}{kT_2}}$$

Substituting $E_a$ = 1.65 eV, $T_1$ = 620 °C or 893 K, $T_2$ = 600 °C or 873 K, $R_2$ = 8 nm/min, and $k/q = \dfrac{1.38x10^{-23}}{1.6x10^{-19}} = 8.625x10^{-5}$ (eV/K)

$$\frac{R_1}{R_2} = e^{\left[\frac{-E_a(T_2-T_1)}{k/q(T_1)(T_2)}\right]}$$

$$\frac{R_1}{8} = e^{\left[\frac{(-1.65)(873-893)}{(8.625x10^{-5})(893)(873)}\right]} = e^{\frac{32.4}{67.2}} = 1.62$$

Therefore, $R_1$ = 13 nm/min.

### 7.2.1 Equipment

The design and operation of CVD reactors depend on a variety of factors. One way of grouping CVD reactors depends on the method used to heat the wafers. Another criterion is the pressure regime of operation (atmospheric-pressure versus reduced-pressure). The reduced-pressure group can be further split into low-pressure CVD reactors in which the energy is entirely thermal as well as plasma-enhanced CVD reactors.

There are four general methods of wafer heating: (1) resistance heating, (2) RF induction heating, (3) heating by energy from a glow discharge (plasma), and (4) heating by photon energy. Energy can be transferred either to the reactant gases or substrate. When radiant heating, from resistance-heated coils surrounding the reaction tube, is utilized, not only the wafer but also the reaction chamber walls become hot, and such designs are termed hot-wall reactors. In these systems, film formation occurs on both the substrate and chamber walls. This implies that they require frequent cleaning to avoid particle contamination. On the other hand, energy input via RF induction or infrared lamps mounted within the reactor only heats the wafers as well as susceptors but does not cause appreciable heating of the chamber walls. They are cold-wall reactors.

For high-volume production, the number of wafers produced per batch should be as large as possible. This requirement has led to the development of hot-wall, low-pressure CVD reactor displayed in ***Figure 7.4***. For maximum wafer capacity, the wafers are held vertically (perpendicular to the gas flow) in a quartz tube and separated from each other by a narrow space. The pressure is typically between 0.1 and 5.0 torr, temperature between 300°C and 900°C, and gas flow rates between 100 and 1000 standard $cm^3$/minute (sccm). Large load space, good uniformity, and the ability to feed large-diameter wafers are the major advantages of this reactor, but low deposition rates and frequent use of special gases can pose practical problems.

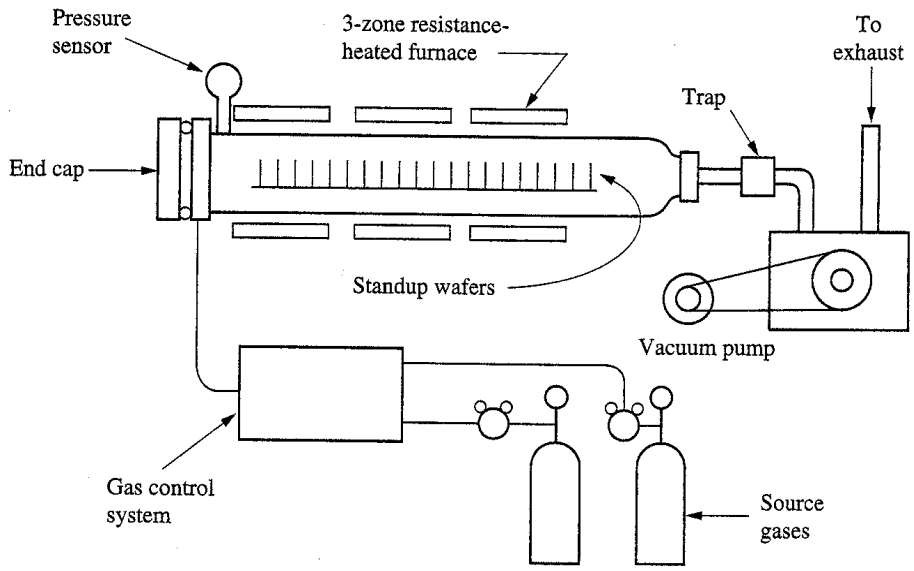


***Figure 7.4***: Schematic of a simple commercial hot-wall, low-pressure reactor for routine, high wafer capacity deposition of polysilicon.

Atmospheric-pressure CVD (APCVD) reactors were the first to be used in the microelectronics industry. Operation at atmospheric pressure keeps reactor design simple and allows high deposition rates. However, the technique is susceptible to gas-phase reactions and the films typically exhibit poor step coverage. Since APCVD is generally conducted in the mass-transport-limited regime, the reactant flux to all parts of the every substrate in the reactor must be precisely controlled. ***Figure 7.5*** shows the schematic of three typical APCVD reactors.

***Figure 7.6*** shows a typical commercial PECVD system. Rather than relying solely on thermal energy to sustain the chemical reactions, PECVD systems uses an RF-induced glow discharge to transfer energy into the reactant gases, allowing the substrate to remain at a lower temperature than that in APCVD and LPCVD. PECVD thus allows the deposition of films on substrates that do not have the thermal stability. In addition, PECVD can enhance the deposition rate as compared with thermal reactions alone and can produce films of unique compositions and properties. However, the limited capacity, especially for large-diameter wafers, and possibility of particle contamination by loosely adhering deposits may be major concerns.

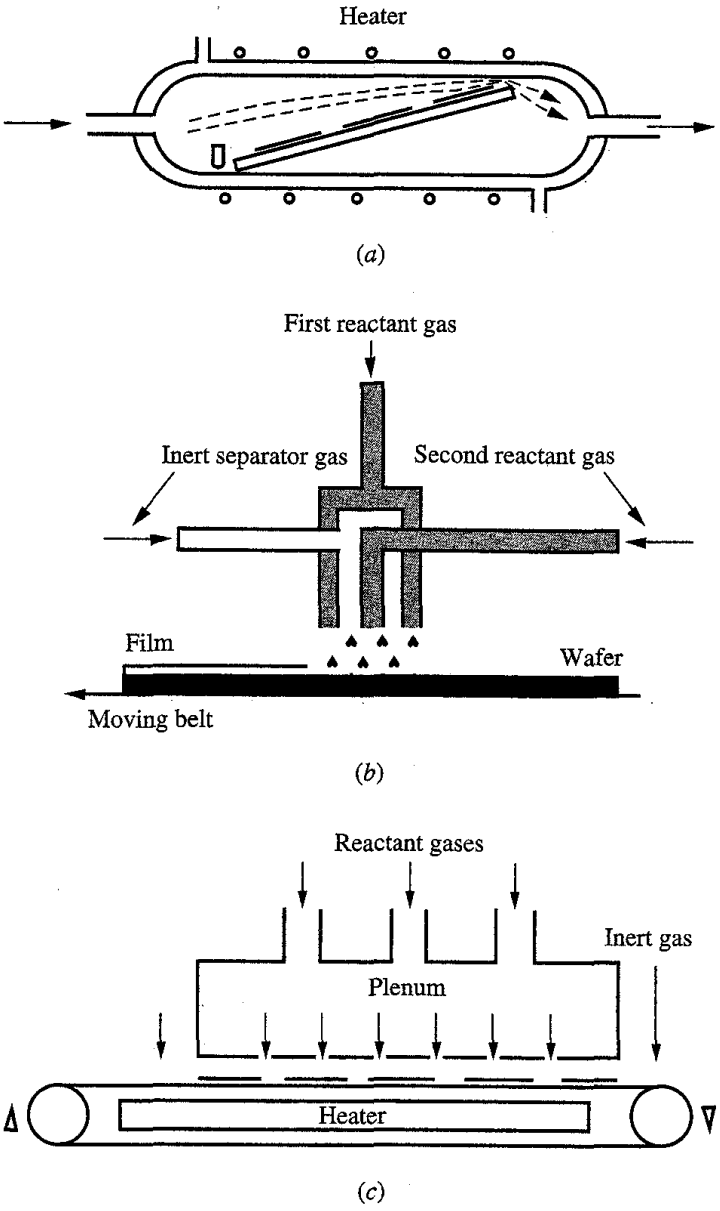


***Figure 7.5***: (a) Horizontal tube APCVD reactor. (b) Gas injection-type continuous-processing APCVD reactor. (c) Plenum-type continuous-processing APCVD reactor.

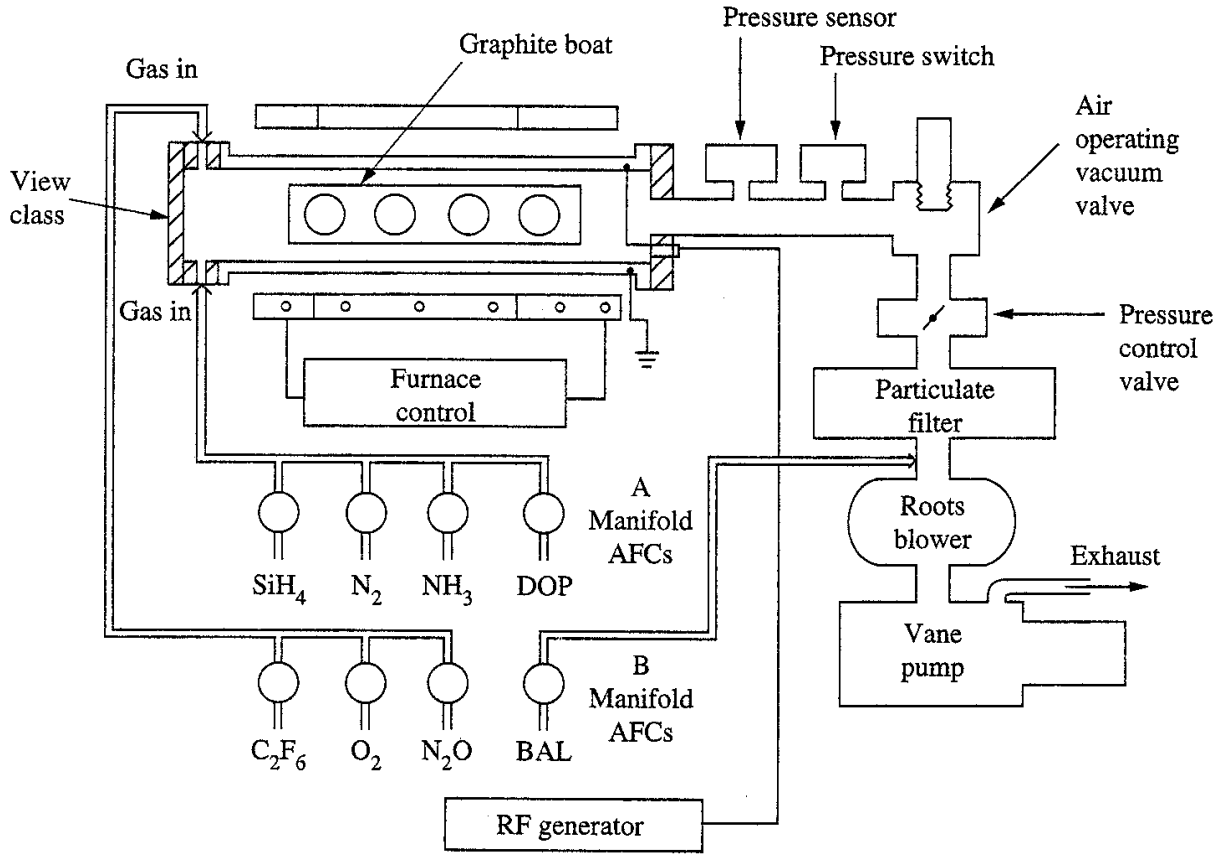


***Figure 7.6***: Schematic of a typical commercial PECVD system.

With regard to PECVD reactors, there are three general types: (1) parallel plate, (2) horizontal tube, and (3) single wafer. In the parallel plate reactor depicted in ***Figure 7.7(a)***, the electrode spacing is typically 5 to 10 cm and the operating pressure is in the range of 0.1 to 5 torr. In spite of the simplicity, the parallel plate system suffers from low throughput for large-diameter wafers. Moreover, particulates flaking off from the walls or the upper electrode can fall on the horizontally positioned wafers.

A horizontal PECVD reactor resembles a hot-wall LPCVD system consisting of a long horizontal quartz tube that is radiantly heated. Special long rectangular graphite plates serve as both the electrodes to establish the plasma and holders of the wafers. The electrode configuration is designed to provide a uniform plasma environment for each wafer to ensure film uniformity. These vertically oriented graphite electrodes are stacked parallel to one another, side by side, with alternating plates serving as power and ground for the RF voltage. The plasma is formed in the space between each pair of plates.

A more recent PECVD reactor is the single-wafer design displayed in ***Figure 7.7***. The reactor, which is load-locked, offers cassette-to-cassette operations and provides rapid radiant heating of each wafers as well as allowing in-situ monitoring of the film deposition. Wafers larger than 200 mm in diameter can be processed.

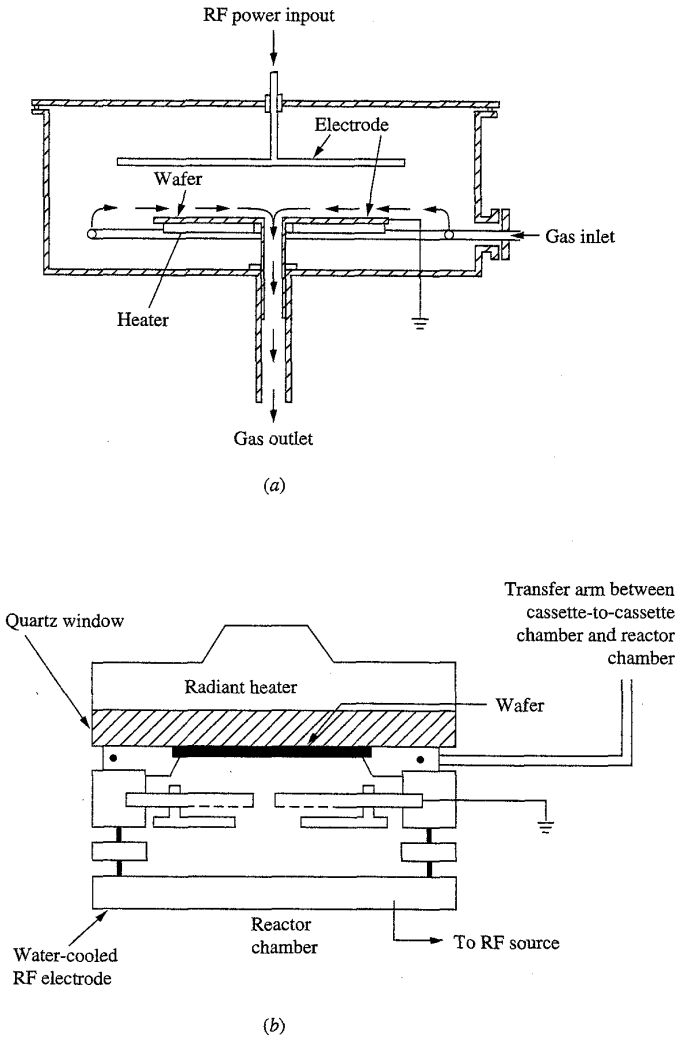


***Figure 7.7***: Schematic diagrams of plasma deposition reactors: (a) parallel plate type, and (b) single-wafer type.

### 7.2.2 Safety Issues

Most of the gases used for film deposition are toxic and these hazardous gases can also cause reactions with the vacuum pump oil. These hazardous gases can be divided into four general classes: pyrophoric (flammable or explosive), poisonous, corrosive, and dangerous combinations of gases. Gases commonly used in CVD are listed in ***Table 7.2***. Gas combinations such as silane with halogens, silane with hydrogen, and oxygen with hydrogen will cause safety problems. In addition, silane reacts with air to form solid products causing particle contamination in the gas lines. These particles can plug the pipes and perhaps create combustion.

***Table 7.2***: Gases commonly used in CVD.

| Gas | Formula | Hazards | Flammable Exposure Limits in air (vol %) | Toxic Limit (ppm) |
|---|---|---|---|---|
| Ammonia | $NH_3$ | Toxic, corrosive | 16-25 | 25 |
| Argon | Ar | Inert | -- | -- |
| Arsine | $AsH_3$ | Toxic | -- | 0.05 |
| Diborane | $B_2H_6$ | Toxic, flammable | 1-98 | 0.1 |
| Dichlorosilane | $SiH_2Cl_2$ | Toxic, flammable | 4-99 | 5 |
| Hydrogen | $H_2$ | Flammable | 4-74 | -- |
| Hydrogen chloride | HCl | Toxic, corrosive | -- | -- |
| Nitrogen | $N_2$ | Inert | -- | -- |
| Nitrogen Oxide | $N_2O$ | Oxidizer | -- | -- |
| Oxygen | $O_2$ | Oxidizer | -- | -- |
| Phosphine | $PH_3$ | Toxic, flammable | Pyrophoric | 0.3 |
| Silane | $SiH_4$ | Toxic, flammable | Pyrophoric | 0.5 |

## 7.3 Polysilicon

Polysilicon is deposited by pyrolyzing silane between 575°C and 650°C in a low-pressure reaction:

$$SiH_4\ (g) \rightarrow\ Si\ (s) + 2H_2\ (gas)$$

Either pure silane or 20 to 30% silane in nitrogen is bled into the LPCVD system at a pressure of 0.2 to 1.0 torr. For practical use, a deposition rate of about 10 to 20 nm/min is required. The properties of the LPCVD polysilicon films are determined by the deposition pressure, silane concentration, deposition temperature, and dopant content.

Amorphous silicon can be prepared by the glow discharge decomposition of silane. Processing parameters such as deposition rate are affected by deposition variables such as the total pressure, reactant partial pressure, discharge frequency and power, electrode materials, gas species, reactor geometry, pumping speed, electrode spacing, and deposition temperature. The higher the deposition temperature and RF power, the higher is the deposition rate.

Polysilicon can be doped by adding phosphine, arsine, or diborane to the reactants (in-situ doping). Adding diborane causes a large increase in the deposition rate because diborane forms borane radicals, $BH_3$, that catalyze gas-phase reactions and increase the deposition rate. In contrast, adding phosphine or arsine causes a rapid reduction in the deposition rate, because phosphine or arsine is strongly adsorbed on the silicon substrate surface thereby inhibiting the dissociative chemisorption of $SiH_4$. Despite the poorer thickness uniformity across a wafer when dopants are incorporated, uniformity can be maintained by controlling precisely the flow of reactant gases around the samples.

Polysilicon can also be doped independently by other methods. ***Figure 7.8*** shows the resistivity of polysilicon doped with phosphorus by diffusion, ion implantation, and in-situ doping. The dopant concentration in diffused polysilicon often exceeds the solid solubility limit, with the excess dopant atoms segregated at the grain boundaries. The high resistivity observed for lightly implanted polysilicon is caused by carrier traps at the grain boundaries. Once these traps are saturated with dopants, the resistivity decreases rapidly and approaches that for implanted single-crystal silicon.

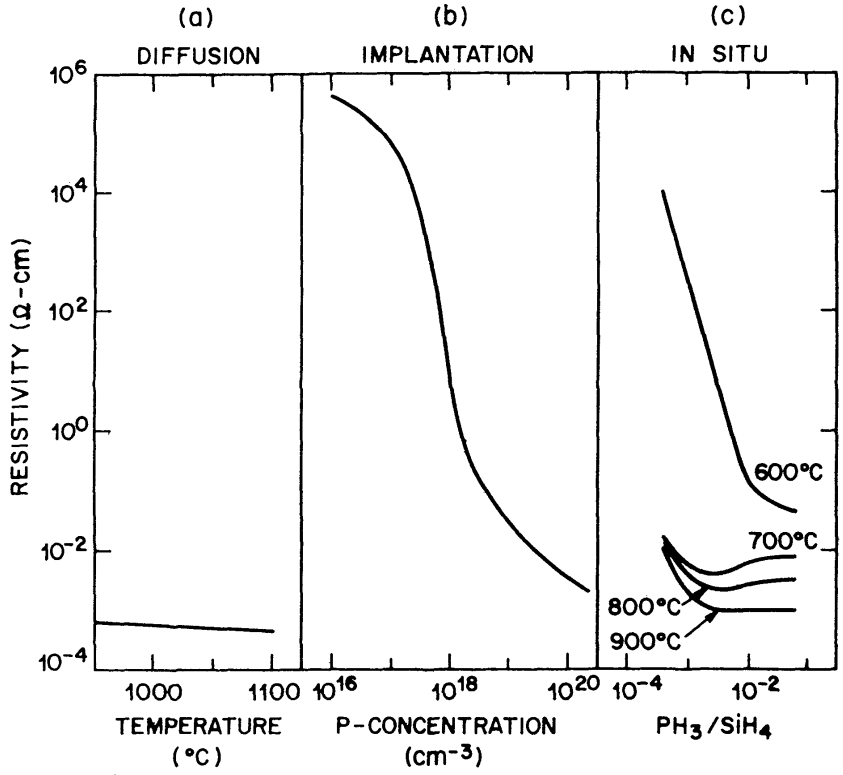


***Figure 7.8***: Resistivity of phosphorus doped polysilicon. (**a**) Diffusion: 1 hour at the indicated temperature. (**b**) Implantation: 1 hour anneal at 1100°C. (**c**) In-situ: as deposited at 600°C and after a 30-minute anneal at the indicated temperature.

Polysilicon can be oxidized in dry oxygen at temperatures between 900°C and 1000°C to form an insulator between the doped polysilicon gate and other conducting layers. The resulting material, semi-insulating polysilicon (SIPOS) is also employed as a passivating coating for high voltage devices.

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## 7.4 Silicon Dioxide

Several deposition methods are used to produce silicon dioxide. Films can be deposited at lower than 500°C by reacting silane, dopant (phosphorus in this example), and oxygen under reduced pressure or atmospheric pressure.

$$SiH_4\ (g) + O_2\ (g) \rightarrow SiO_2\ (s) + 2H_2\ (g)$$

$$4PH_3\ (g) + 5O_2\ (g) \rightarrow 2P_2O_5\ (s) + 6H_2\ (g)$$

The process can be conducted in an APCVD or LPCVD chamber. The main advantage of silane-oxygen reactions is the low deposition temperature allowing films to be deposited over aluminum metallization. The primary disadvantages are poor step coverage and high particle contamination caused by loosely adhering deposits on the reactor walls.

Silicon dioxide can be deposited at 650°C to 750°C in an LPCVD reactor by pyrolyzing tetraethoxysilane, $Si(OC_2H_5)_4$. This compound, abbreviated TEOS, is vaporized from a liquid source. The reaction is

$$Si(OC_2H_5)_4\ (l) \rightarrow SiO_2\ (s) + \text{by-products}\ (g)$$

The by-products are organic and organosilicon compounds. LPCVD TEOS is often used to deposit the spacers beside the polysilicon gates. The process offers good uniformity and step coverage, but the high temperature limits its application on aluminum interconnects.

Silicon dioxide can also be deposited by LPCVD at about 900°C by reacting dichlorosilane with nitrous oxide:

$$SiCl_2H_2\ (g) + 2N_2O\ (g) \rightarrow SiO_2\ (s) + 2N_2\ (g) + 2HCl\ (g)$$

This deposition technique provides excellent uniformity, and like LPCVD TEOS, it is employed to deposit insulating layers over polysilicon. However, this oxide is frequently contaminated with small amounts of chlorine that may react with polysilicon causing film cracking.

Plasma-assisted CVD requires the control and optimization of the RF power density, frequency, and duty cycle in addition to the conditions similar to those of an LPCVD process such as gas composition, flow rate, deposition temperature, and pressure. Like the LPCVD process at low temperature, the PECVD process

is surface-reaction-limited, and adequate substrate temperature control is thus necessary to ensure film thickness uniformity.

By reacting silane and oxygen or nitrous oxide in plasma, silicon dioxide films can be formed by the following reactions:

$$SiH_4\ (g) + O_2\ (g) \rightarrow SiO_2\ (s) + 2H_2\ (g)$$

$$SiH_4\ (g) + 4N_2O\ (g) \rightarrow SiO_2\ (s) + 4N_2\ (g) + 2H_2O\ (g)$$

### 7.4.1 Step Coverage and Reflow

Three general types of step coverage are observed for deposited silicon dioxide, as schematically diagrammed in ***Figure 7.9***. A completely uniform or conformal step coverage depicted in ***Figure 7.9a*** results when reactants or reactive intermediates adsorb and then migrate promptly along the surface before reacting. When the reactants adsorb and react without significant surface migration, the deposition rate is proportional to the arrival angle of the gas molecules. ***Figure 7.9b*** illustrates an example in which the mean free path of the gas is much larger than the dimensions of the step. The arrival angle in two dimensions at the top horizontal surface is 180°. At the top of the vertical step, the arrival angle is only 90°, and so the film thickness is halved. Along the vertical walls, the arrival angle, $\phi$, is determined by the width of the opening, $w$, and the distance from the top, $z$:

$$\phi = \arctan\ (w / z) \qquad \textit{(Equation 7.2)}$$

This type of step coverage is thin along the vertical walls and may have a crack at the bottom of the step caused by self-shadowing. ***Figure 7.9c*** depicts the situation where there is minimal surface mobility and the mean free path is short. Here the arrival angle at the top of the step is 270°, thus giving a thicker deposit. The arrival angle at the bottom of the step is only 90°, and so the film is thin. The thick cusp at the top of the step and the thin crevice at the bottom combine to give a re-entrant shape that is particularly difficult to cover with metal.

Doped oxides used as diffusion sources contain 5 to 15 weight % of the dopant. Doped oxides for passivation or interlevel insulation contain 2 to 8 wt. % phosphorus to prevent the diffusion of ionic impurities to the device. Phosphosilicate glass (PSG) used for the reflow process contains 6 to 8 wt. % phosphorus. Oxides with lower phosphorus concentrations will not soften and

flow, but higher phosphorus concentrations can give rise to deleterious effects for phosphorus can react with atmospheric moisture to form phosphoric acid which can consequently corrode the aluminum metallization. The addition of boron to PSG further reduces the reflow temperature without exacerbating this corrosion problem. Borophosphosilicate glass (BPSG) typically contains 4 to 6 wt. % P and 1 to 4 wt. % B.

Poor step coverage of PSG or BPSG can be corrected by heating the samples until the glass softens and flow. PSG reflow is illustrated by the scanning electron micrographs shown in ***Figure 7.10*** and ***Figure 7.11***. Reflow is manifested by the progressive loss of detail.

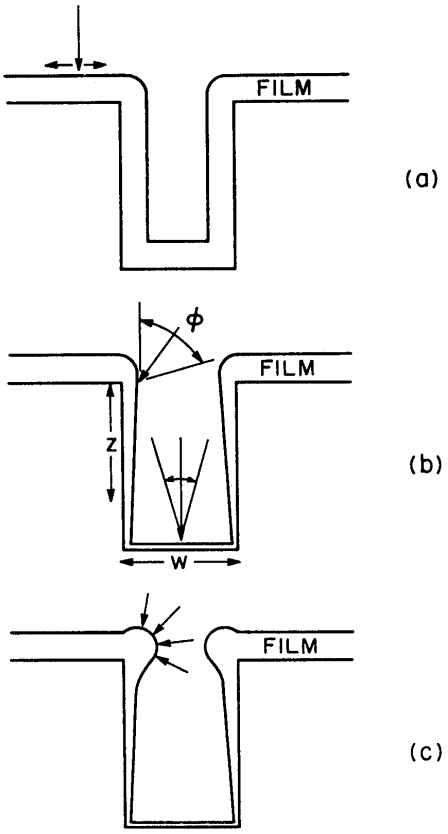


***Figure 7.9***: Step coverage of deposited films. (**a**) Uniform coverage resulting from rapid surface migration. (**b**) Nonconformal step coverage for long mean free path and no surface migration. (**c**) Nonconformal step coverage for short mean free path and no surface migration.

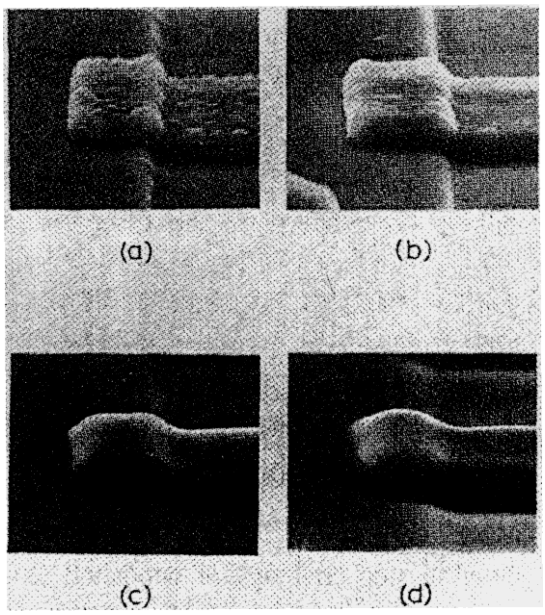


***Figure 7.10***: SEM photographs (3200x) showing surfaces of 4.6 wt. % P-glass annealed in steam at 1100°C for the following times: (**a**) 0 min; (**b**) 20 min; (**c**) 40 min; (**d**) 60 min.

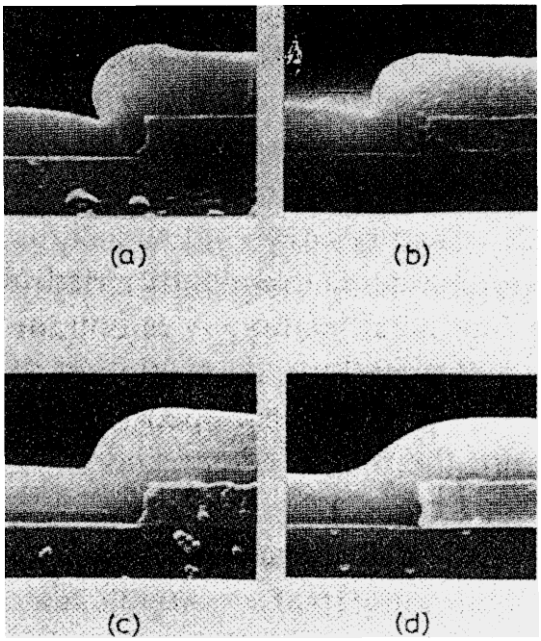


***Figure 7.11***: SEM cross sections (10,000x) of samples annealed in steam at 1100°C for 20 minutes for the following weight percent of phosphorus: (**a**) 0.0 wt. % P; (**b**) 2.2 wt. % P; (**c**) 4.6 wt. % P; (**d**) 7.2 wt. % P.

The step coverage of deposited oxides can be improved by planarization or etch-back techniques. ***Figure 7.12*** illustrates the planarization process. Since the organic resist material has a low viscosity, reflow occurs during application or the subsequent bake. The sample is then plasma etched to remove all the organic coating and part of the PSG, as long as the etching conditions are selected to remove the organic material and PSG at equal rates.

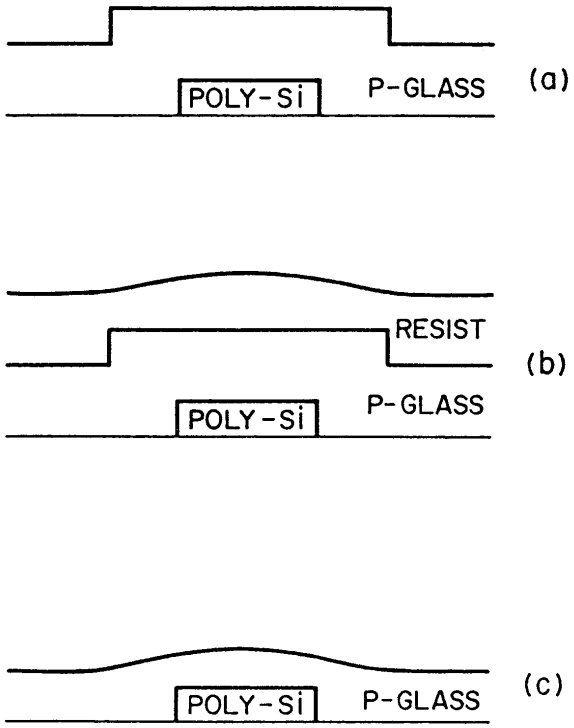


***Figure 7.12***: Schematic representation of the planarization process. (**a**) Polysilicon step covered with P-glass. (**b**) Coated with resist. (**c**) After etching the resist leaving a smooth P-glass surface.

Chapter 7

## 7.5 Silicon Nitride

Stoichiometric silicon nitride ($Si_3N_4$) can be deposited at 700°C to 800°C at atmospheric pressure:

$$3SiH_4\ (g) + 4NH_3\ (g) \rightarrow Si_3N_4\ (s) + 12H_2\ (g)$$

Using LPCVD, silicon nitride can be produced by reacting dichlorosilane and ammonia at temperature between 700°C and 800°C:

$$3SiCl_2H_2\ (g) + 4NH_3\ (g) \rightarrow Si_3N_4\ (s) + 6H_2\ (g)$$

The reduced-pressure technique has the advantage of yielding good uniformity and higher wafer throughput.

Hydrogenated silicon nitride films can be deposited by reacting silane and ammonia or nitrogen in plasma at reduced temperature:

$$SiH_4\ (g) + NH_3\ (g) \rightarrow\ SiN:H\ (s) + 3H_2\ (g)$$

$$SiH_4\ (g) + N_2\ (g) \rightarrow\ 2SiN:H\ (s) + 3H_2\ (g)$$

Plasma-assisted deposition yields films at low temperature by reacting the gases in a glow discharge. Two plasma deposited materials, plasma deposited silicon nitride (SiNH) and plasma deposited silicon dioxide, are useful in VLSI. On account of the low deposition temperature, 300°C to 350°C, plasma nitride can be deposited over the final device metallization. Plasma-deposited films contain large amounts of hydrogen (10 to 35 atomic %). Hydrogen is bonded to silicon as Si-H, to nitrogen as N-H, and to oxygen as Si-OH and $H_2O$. ***Table 7.3*** displays some of the properties of silicon nitride films fabricated using LPCVD and plasma-assisted deposition.

***Table 7.3***: Properties of silicon nitride films.

| Deposition | LPCVD | Plasma |
|---|---|---|
| Temperature ($^oC$) | 700-800 | 250-350 |
| Composition | $Si_3N_4$ (H) | $SiN_xH_y$ |
| Si/N ratio | 0.75 | 0.8-1.2 |
| Atom % H | 4-8 | 20-25 |
| Refractive index | 2.01 | 1.8-2.5 |
| Density ($g/cm^3$) | 2.9-3.1 | 2.4-2.8 |
| Dielectric constant | 6-7 | 6-9 |
| Resistivity (ohm-cm) | $10^{16}$ | $10^6$-$10^{15}$ |
| Dielectric strength ($10^6$V/cm) | 10 | 5 |
| Energy gap (eV) | 5 | 4-5 |
| Stress ($10^9$ dyne/$cm^2$) | 10T | 2C-5T |

## 7.6 Rapid Thermal Chemical Vapor Deposition (RTCVD)

The application of rapid thermal processing (RTP) to CVD processes is particularly well suited to single-wafer cluster tool technology. A typical design of an RTCVD system is displayed in ***Figure 7.13***. The chamber walls are water-cooled thus eliminating deposition on the chamber walls. RTCVD requires higher temperature but shorter time to deposit the same material compared to LPCVD. Furthermore, temperature is the switch that turns the RTP deposition process on or off, avoiding the long ramp-up and ramp-down times required in conventional methods.

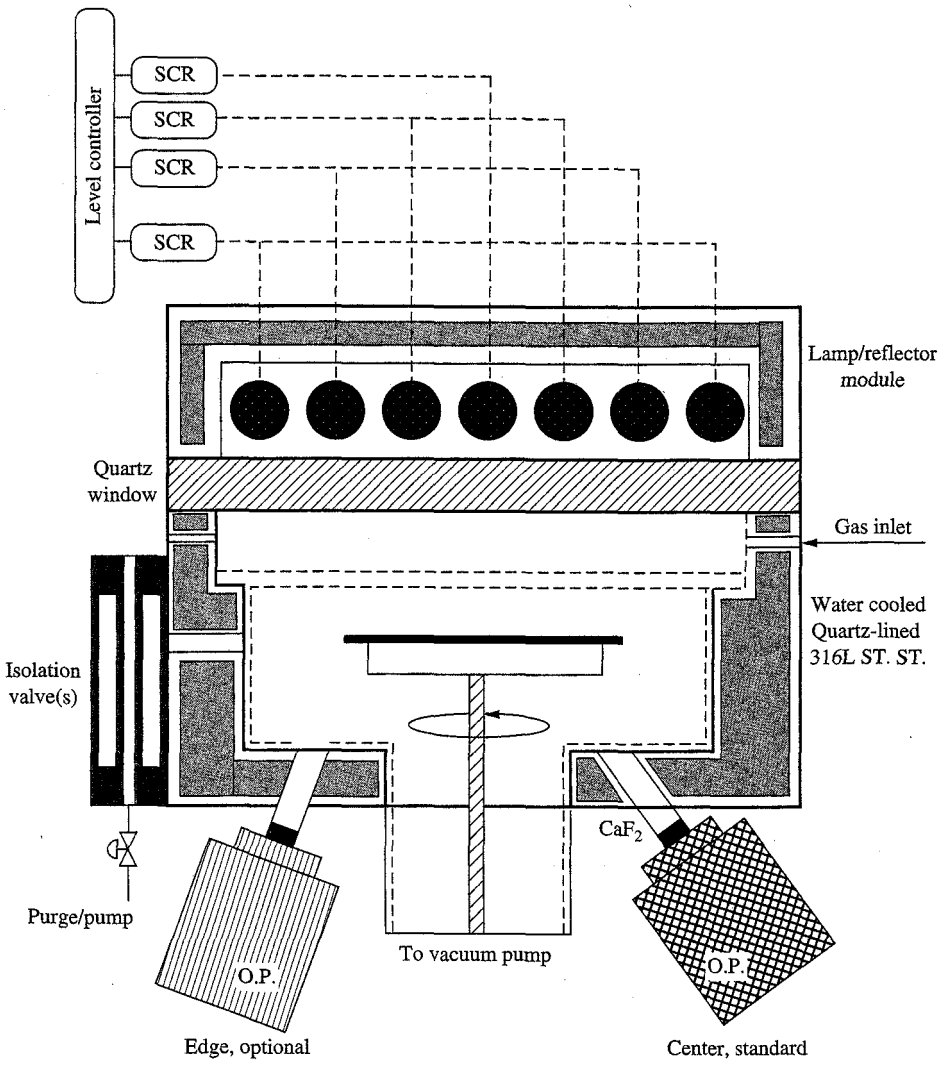


***Figure 7.13***: Cross-sectional view of a RTCVD chamber.

To be commercially viable, RTCVD systems must be able to process a single wafer in 1 to 2 minutes, giving a corresponding throughput of 30 to 60 wafers per

hour. For relatively thick deposited films of 100 to 200 nm, this requires deposition rates greater than 100 nm/min. In comparison, the typical deposition rate in conventional batch LPCVD processes is about 10 nm/min.

As an example, $SiO_2$ layers with thickness of several hundred nanometers serve as inter-level dielectric between metallization layers or as a sidewall spacer on a polysilicon gate. An important requirement is good oxide step coverage, and as aforementioned, the physical parameter indicative of step coverage is surface diffusion. This requirement favors the use of TEOS and TMCTS (tetramethylcyclotrasiloxane) in the process. The RTCVD of $SiO_2$ by pyrolysis of TEOS is believed to occur by the reaction:

$$Si(OC_2H_5)_4 \rightarrow SiO_2\,(s) + 2H_2O + 4C_2H_4$$

Below 800°C, the deposition rate is controlled by surface reaction processes with activation energy of 3.3 eV. This large sensitivity to temperature thus demands tight temperature control for thin oxide deposition at low temperature. Above 800°C, the deposition rate of $SiO_2$ approaches 100 nm/min with a lower activation energy, which meets the throughput and deposition control requirements of the RTCVD system. The high operating temperature makes it infeasible for back end steps in multilevel-metallization technologies that use aluminium.

Thin oxide applications include in-situ deposition of MOS gate structures where Si surface cleaning, gate oxide formation, and polysilicon gate electrode deposition would all occur in a low-pressure, multi-chamber cluster tool. RTCVD yields high-quality films through the use of ultraclean gases in a chamber with a highly regulated ambient, and examples of these reactions are:

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$$

$$SiH_4 + 2N_2O \rightarrow SiO_2 + 2N_2 + 2H_2O$$

$$3SiH_2Cl_2 + 10NH_3 \rightarrow Si_3N_4 + 6NH_4Cl + 6H_2$$

$$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$$

$$SiH_4 \rightarrow Si + 2H_2$$