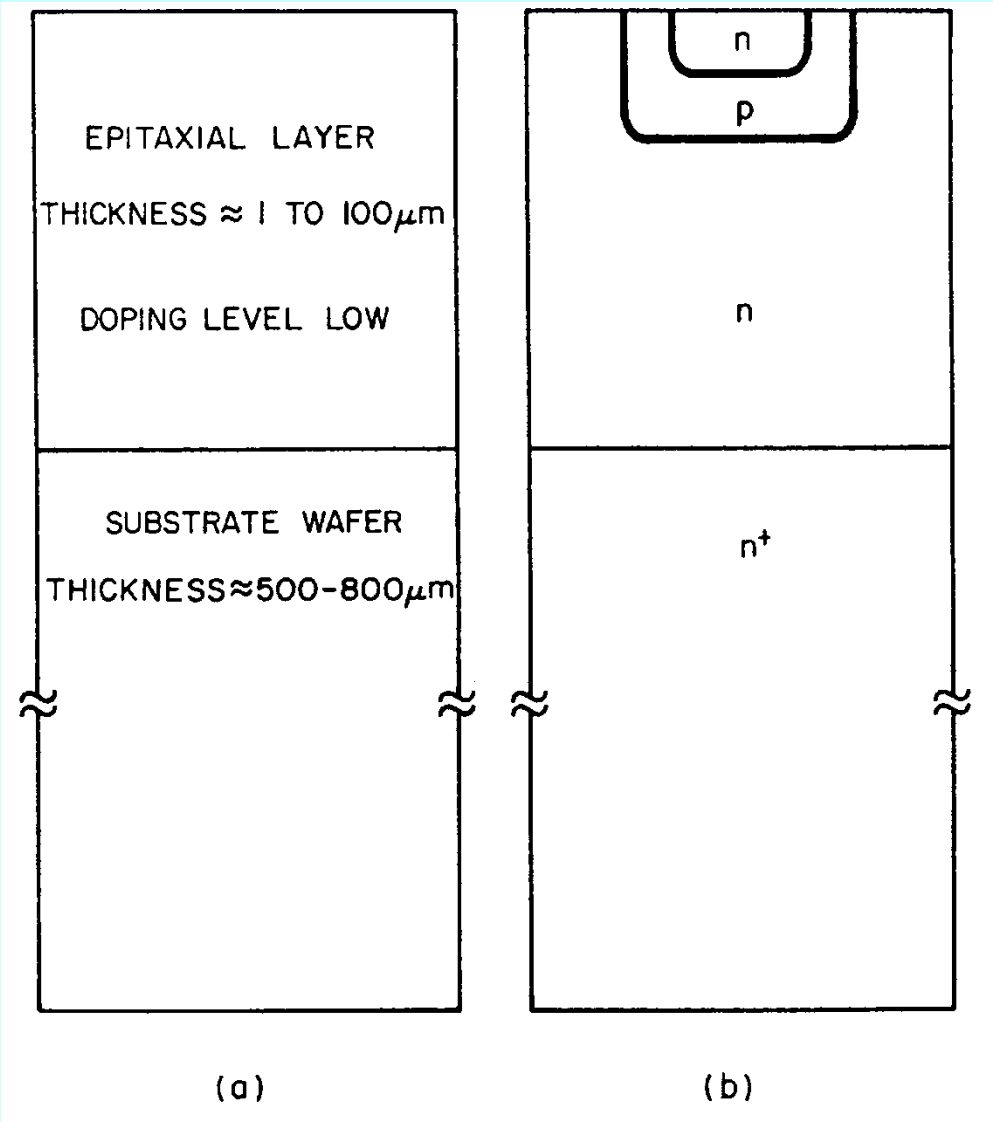
Chapter 3

Epitaxy

Professor Paul K. Chu

Epitaxy (***epi*** means "upon" and ***taxis*** means "ordered") is a term applied to processes used to grow a thin crystalline layer on a crystalline substrate. The seed crystal in epitaxial processes is the substrate. Unlike the Czochralski process, crystalline thin films can be grown below the melting point using techniques such as chemical vapor deposition (CVD), molecular beam epitaxy (MBE), etc.

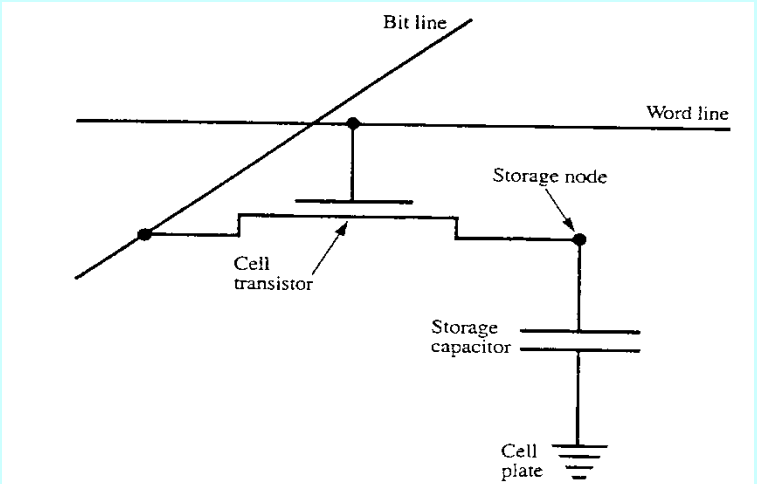
When a material is grown epitaxially on a substrate of the same material, the process is called **homoepitaxy**. On the contrary, if the layer and substrate are of different materials, such as $Al_xGa_{1-x}As$ on GaAs, the process is termed **heteroepitaxy**. Naturally, in heteroepitaxy, the crystal structures of the layer and the substrate must be similar in order to achieve good crystalline integrity.



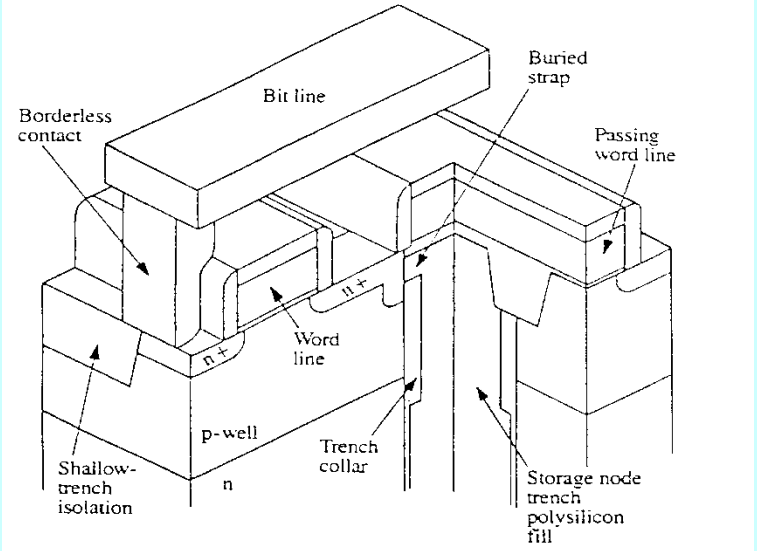
Advantages of epitaxy:

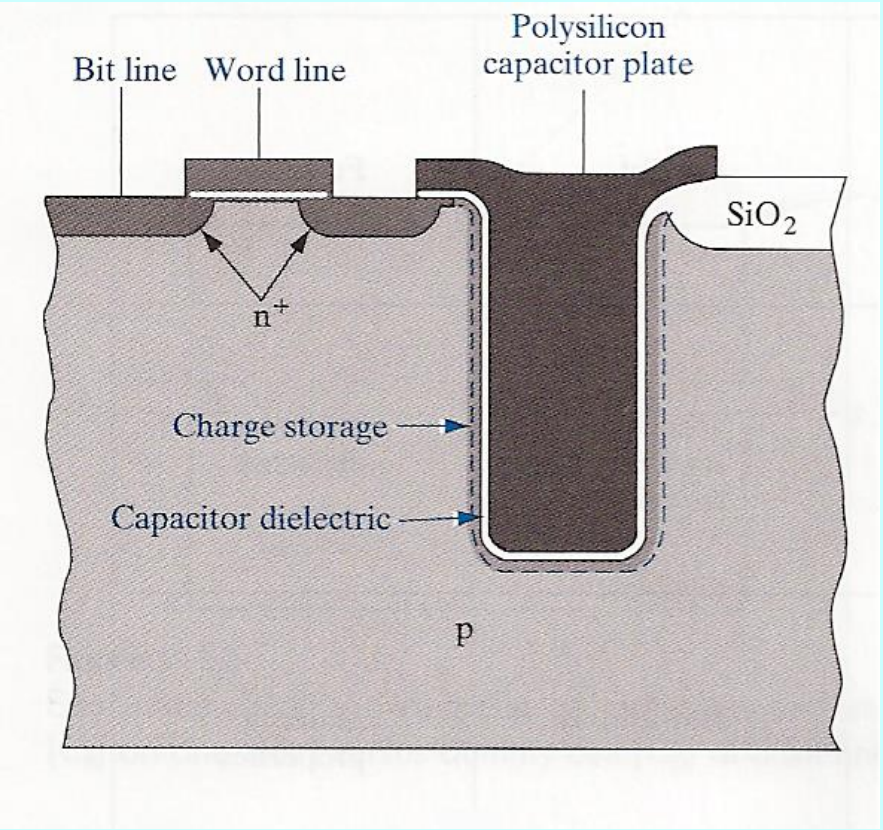
(1) Doping profiles that are not attainable through other conventional means such as diffusion or ion implantation

(2) Physical and chemical properties of the epitaxial layers can be made different from the bulk materials.



256Mbit DRAM (buried strap trench)



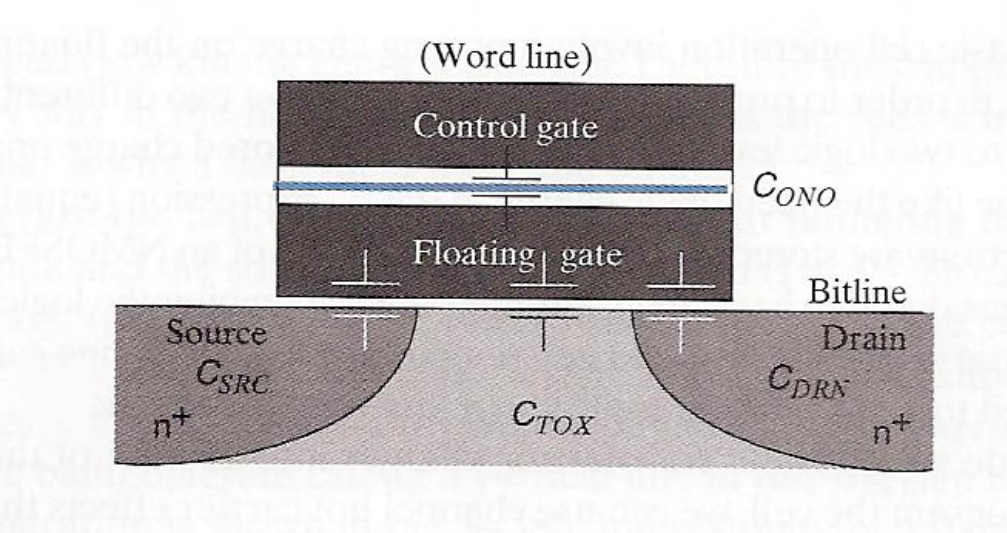


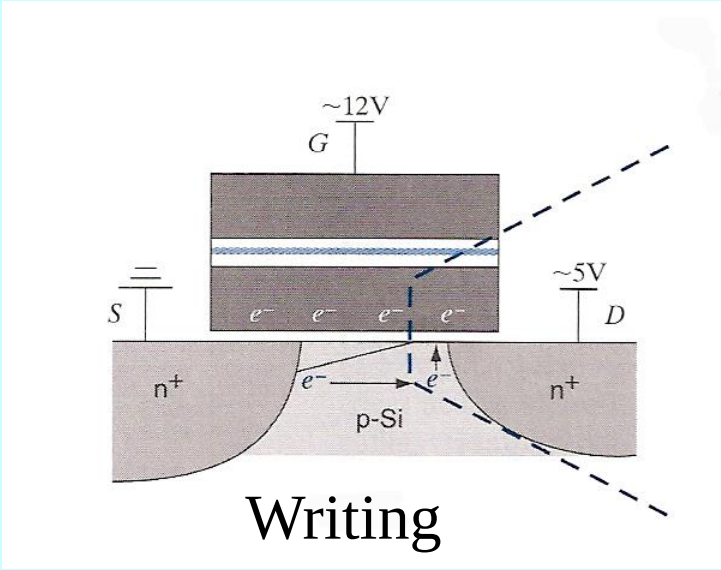
Cross section of a trench DRAM

Alpha-particles originating from packaging materials and the environment can cause electron-hole pairs in the bulk of the wafer. If these charges migrate to the storage cell of a DRAM (dynamic random access memory) structure, the data stored can be wiped out.

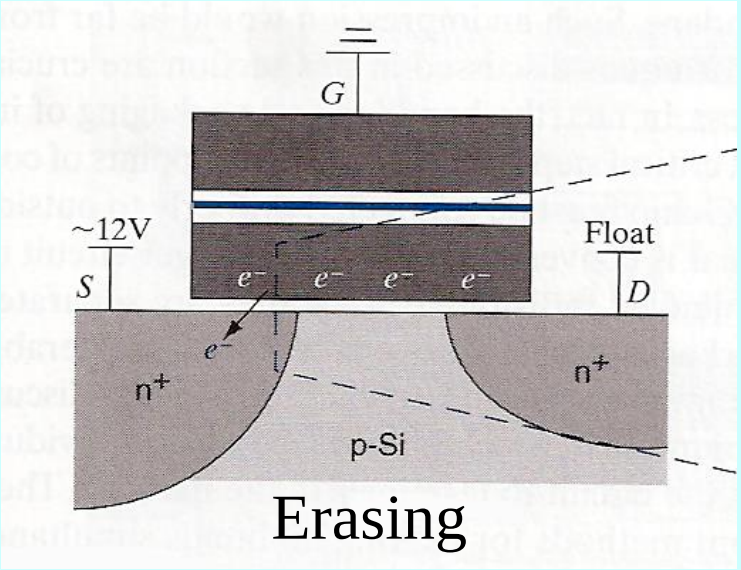
A heavily doped substrate increases the rate of electron-hole pair recombination and the DRAM is less prone to alpha-particle soft errors.

Non-Volatile Flash Memory



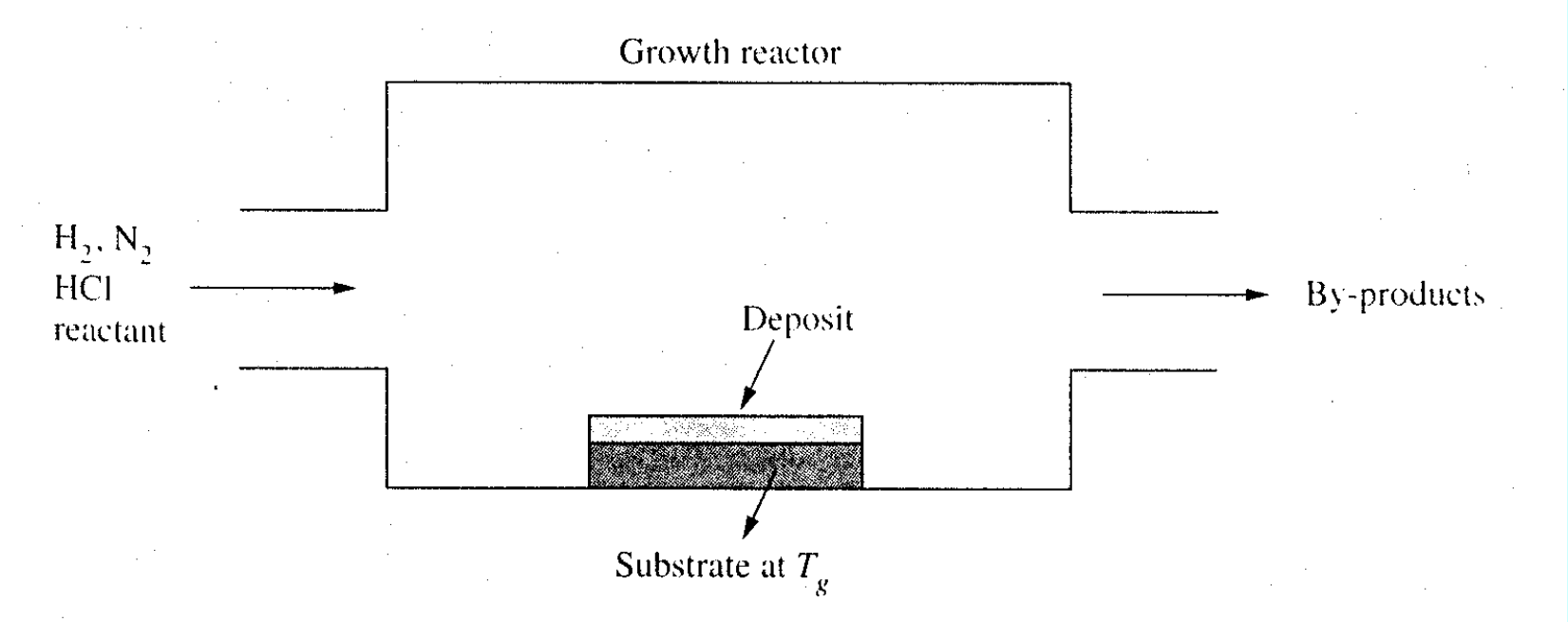


Writing

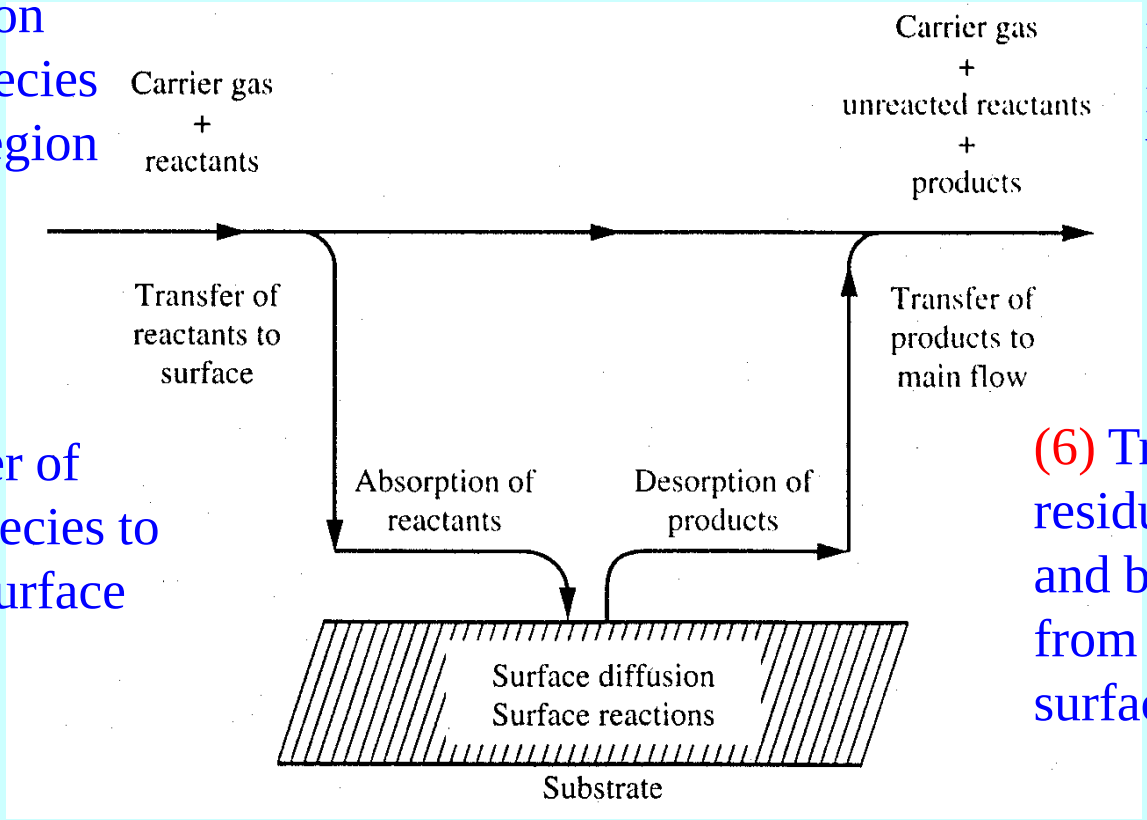


Erasing

Vapor Phase Epitaxy



(1) Introduction of reactant species to substrate region



(2) Transfer of reactant species to substrate surface

(3) Adsorption of reactant species on substrate surface

(4) Surface diffusion, site accommodation, chemical reaction, and layer deposition

(5) Desorption of residual reactants and by-products

(6) Transfer of residual reactants and by-products from substrate surface

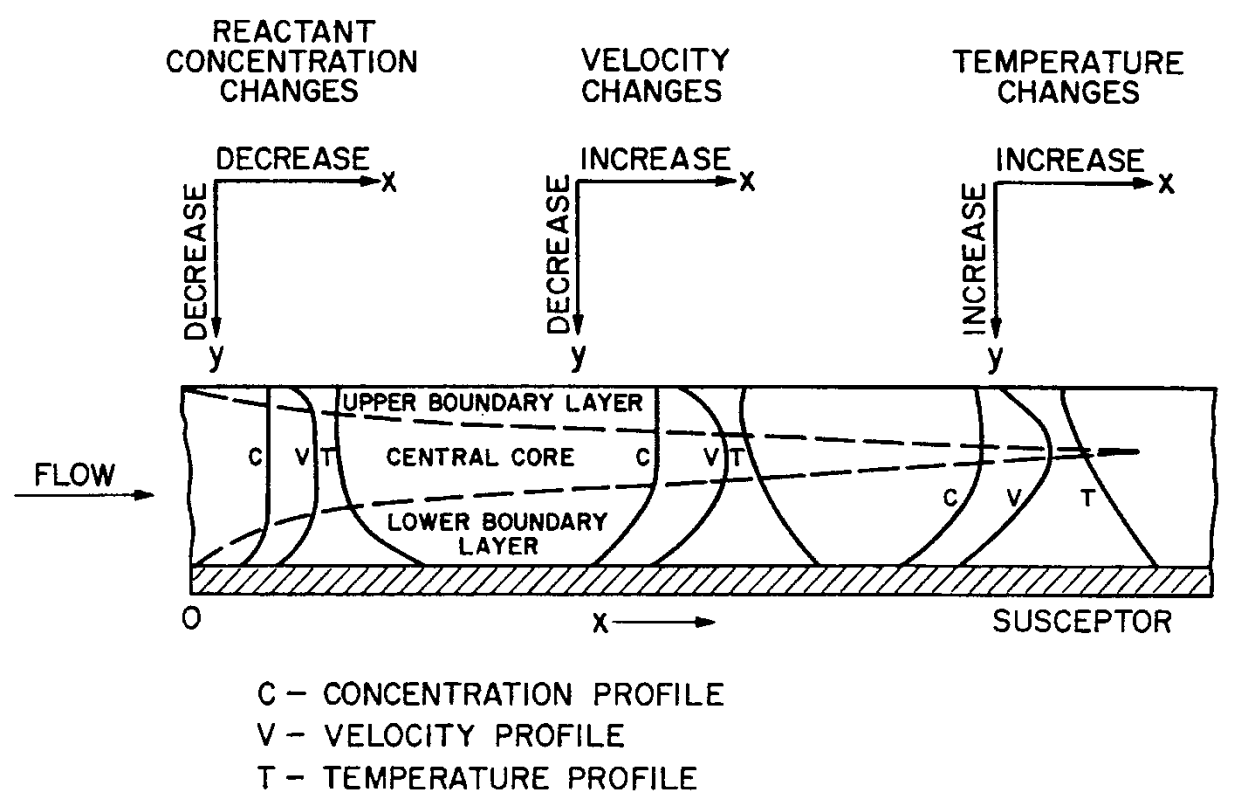
(7) Removal of residual reactants and by-products from the substrate region

The Reynolds number, R_e, characterizes the type of fluid flow in a reactor:

$$R_e = D_r v \rho / \mu$$

where D_r denotes the diameter of the reaction tube, v is the gas velocity, ρ represents the gas density, and μ stands for the gas viscosity. Values of D_r and v are generally several centimeters and tens of cm/s, respectively. The carrier gas is usually H_2, and using typical values for ρ and μ, the value of R_e is about 100. These parameters result in gas flow in the laminar regime. That is, the gases flow in a regular, continuous, and non-turbulent mode and in a specific direction. Accordingly, a boundary layer of reduced gas velocity will form above the susceptor and at the walls of the reaction chamber. The thickness of the boundary layer, y, is defined as: $y = \left[\frac{D_r x}{R_e}\right]^{1/2}$ where x is the distance along the reactor.

Boundary Layer Formation (Horizontal Reactor)



Reactants are transported to the substrate surface and reaction by-products diffuse back into the main gas stream across the boundary layer

The fluxes of species going to and coming from the wafer surface are complex functions of the temperature, pressure, reactant, concentration, layer thickness, etc. By convention, the flux, ***J***, is defined to be the product of ***D*** and ***dn/dy***, and is approximated as:

$$J = \frac{D(n_g - n_s)}{y}$$

where n_g and n_s are the gas stream and surface reactant concentrations, respectively, ***D*** is the gas-phase diffusivity, which is function of pressure and temperature, ***y*** is the boundary layer thickness, and ***J*** is the reactant flux of molecules per unit area per unit time.

In steady state, the reactant flux across the boundary layer is equal to the chemical reaction rate, k_s, at the specimen surface. Therefore,

$$J = k_s n_s \qquad \text{and} \qquad n_s = \frac{n_g}{1 + \frac{k_s y}{D}}$$

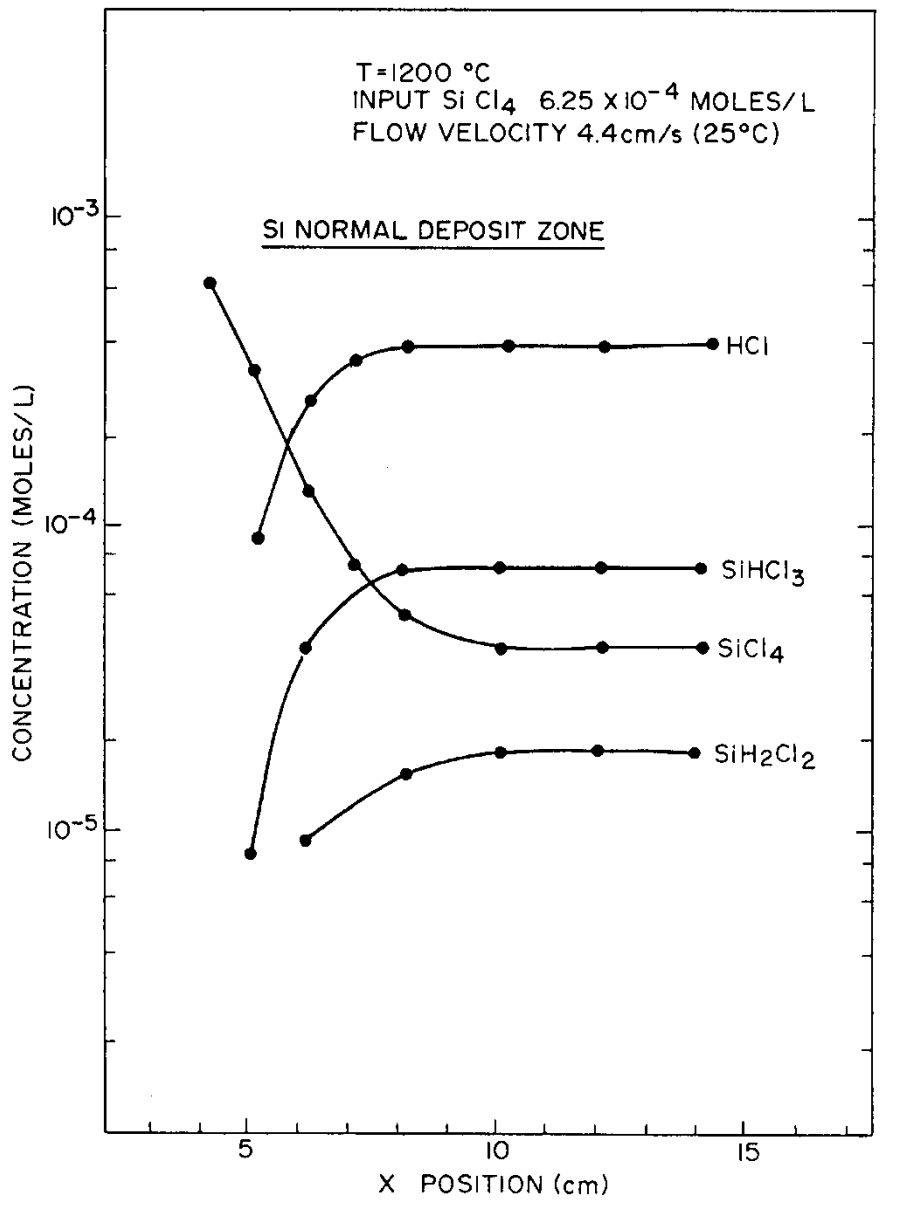
The quantity D/y is called the gas phase mass-transfer coefficient, h_g.

In the limiting case when $k_s >> h_g$, n_s approaches zero, thereby implying that the overall reaction is limited by transport of reactant across the boundary layer. Conversely, if $k_s << h_g$, n_s is roughly equal to n_g, and the growth process will be dominated by the surface chemical reaction rate.

Growth Chemistry

The most common starting chemical is silicon tetrachloride ($SiCl_4$) as it has a lower reactivity with respect to oxidizers in the carrier gas than the other silicon hydrogen chloride compounds, such as SiH_4, $SiHCl_3$, etc. The overall reaction is:

$SiCl_4$ (gas) + $2H_2$ (gas) $\Leftrightarrow$ Si (solid) + 4HCl (gas)



Experimental results indicate the presence of many intermediate chemical species. In particular, at a reaction temperature of 1200°C, four species have been observed using FTIR.

The detailed reaction mechanism is postulated to be:

$$SiCl_4 + H_2 \Leftrightarrow SiHCl_3 + HCl$$

$$SiHCl_3 + H_2 \Leftrightarrow SiH_2Cl_2 + HCl$$

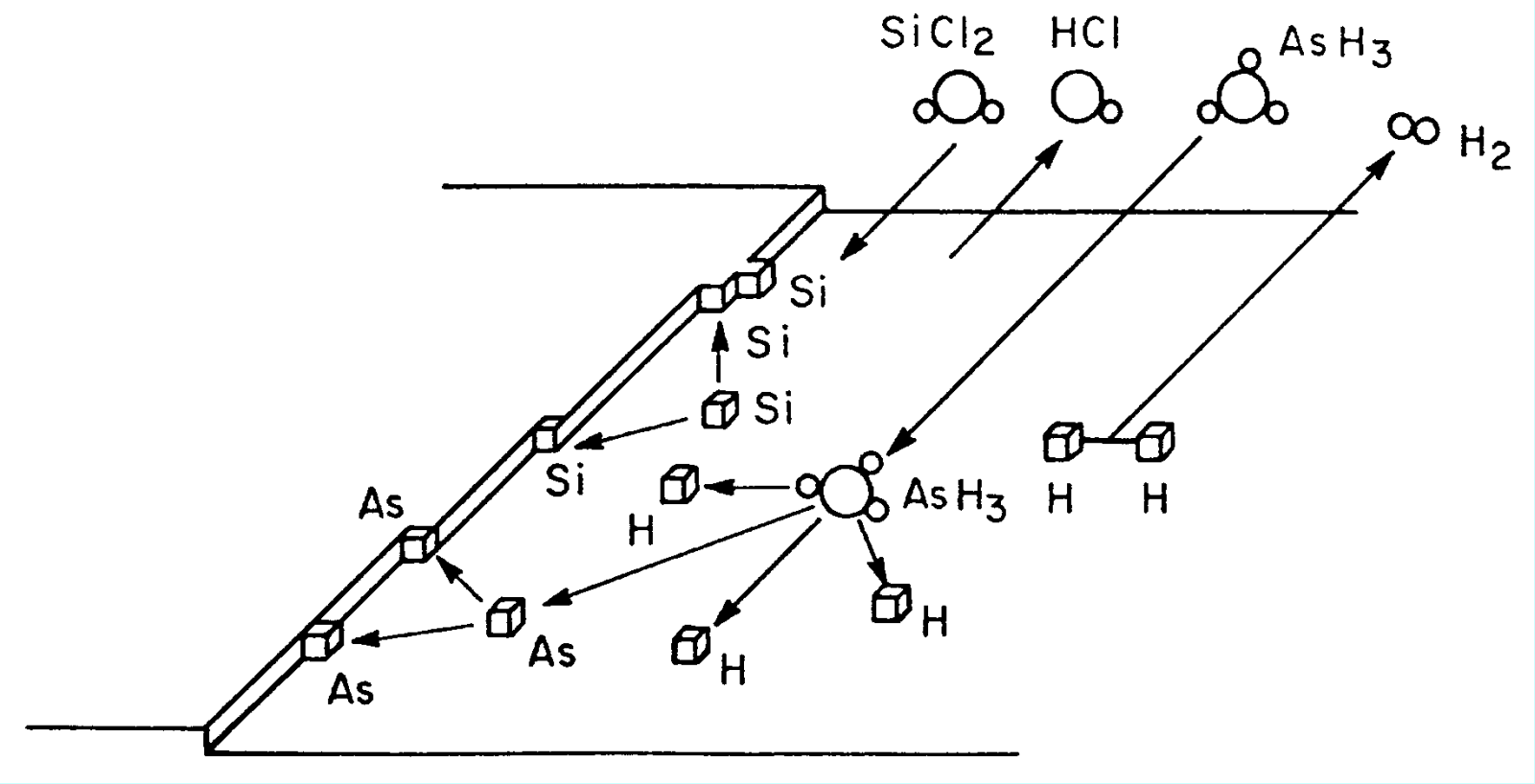
$$SiH_2Cl_2 \Leftrightarrow SiCl_2 + H_2$$

$$SiHCl_3 \Leftrightarrow SiCl_2 + HCl$$

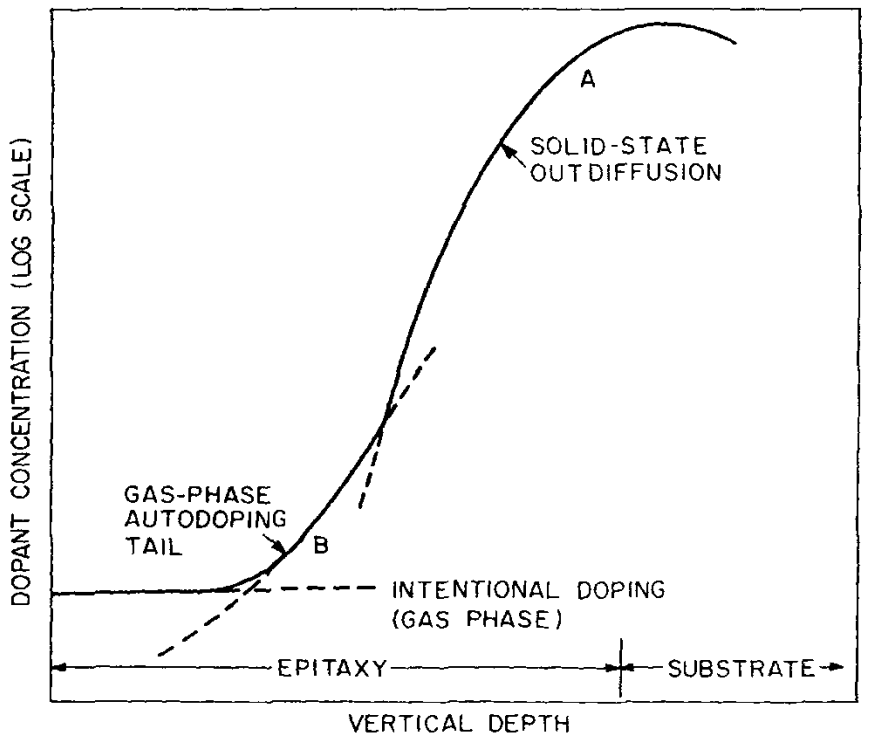
$$SiCl_2 + H_2 \Leftrightarrow Si + 2HCl$$

These reactions are reversible and under certain conditions, the overall reaction rate can become negative. That is, etching occurs in lieu of deposition

Doping



Autodoping



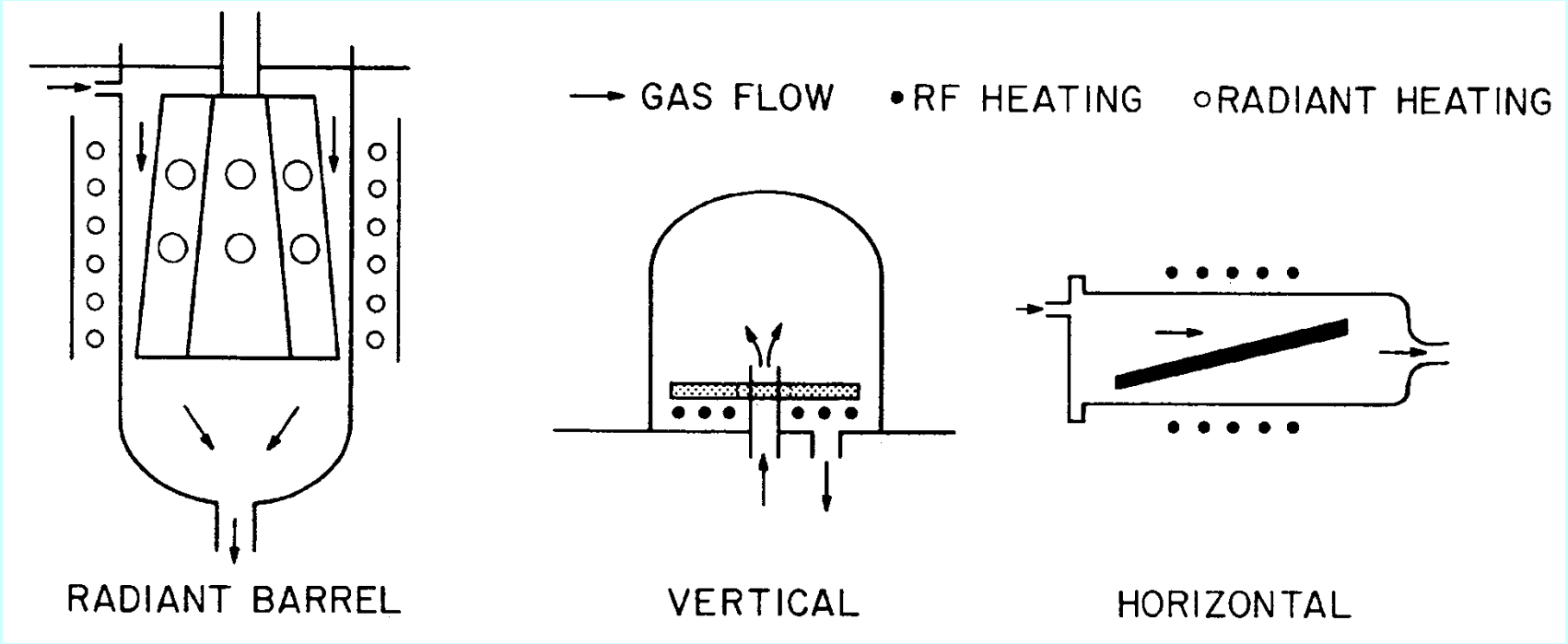
Zone A is due to solid-state out-diffusion from the substrate, and can be approximated by the complementary error function if the growth velocity is less than $2(D/t)^{1/2}$, where D is the dopant diffusion constant and t denotes the deposition time.

When autodoping diminishes, the intentional doping predominates and the profile becomes flat.

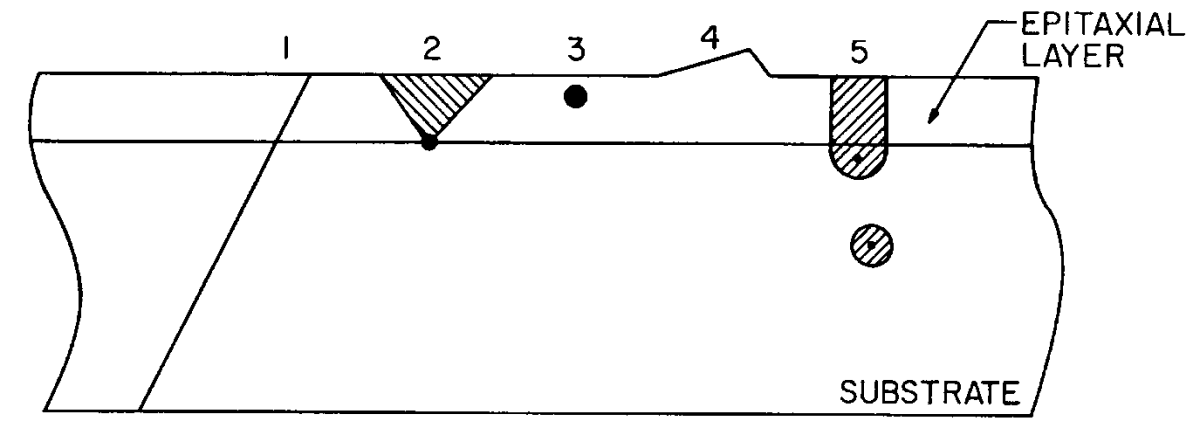
Zone B originates from gas-phase autodoping. Because the dopant evaporating from the wafer surface is supplied from the wafer interior by solid-state diffusion, the flux of dopant from an exposed surface decreases with time.

Autodoping thus limits the minimum layer thickness that can be grown with controlled doping as well as the minimum dopant level.

Reactors


GAS FLOW
RF HEATING
RADIANT HEATING
RADIANT BARREL
VERTICAL
HORIZONTAL

Defects



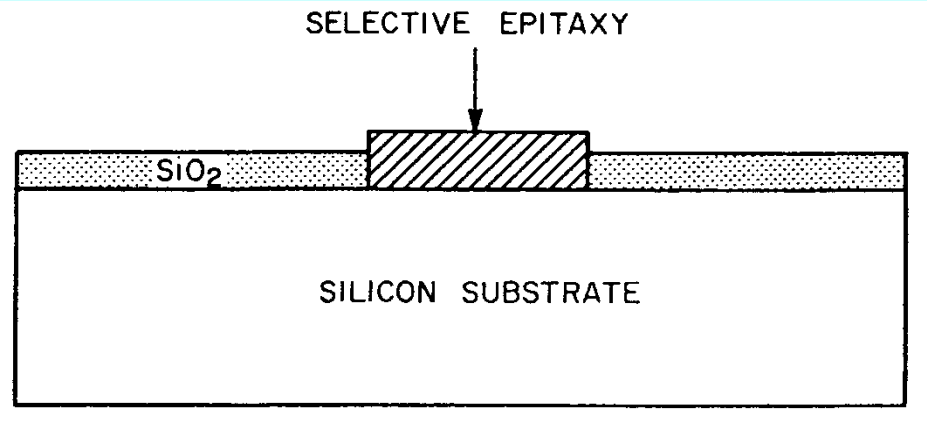
(1) Line (or edge) dislocation initially present in the substrate and extending into the epitaxial layer
(2) Epitaxial stacking fault nucleated by an impurity precipitate on the substrate surface
(3) Impurity precipitate caused by epitaxial process contamination
(4) Growth hillock
(5) Bulk stacking faults, one of which intersects the substrate surface, thereby being extended into the layer

The crystal perfection of an epitaxial layer never exceeds that of the substrate and is frequently inferior.

Generally, defects can be reduced by a higher growth temperature, reduced gas pressure, lower growth rate, and cleaner substrate surface.

A typical pre-epitaxy substrate cleaning process consists of a wet clean followed by a dilute HF dip and an in-situ HCl, HF, or SF_6 vapor etch.

Selective Epitaxy Growth (SEG)



Selective epitaxy is a technique by which single-crystal silicon is fabricated in a small designated area

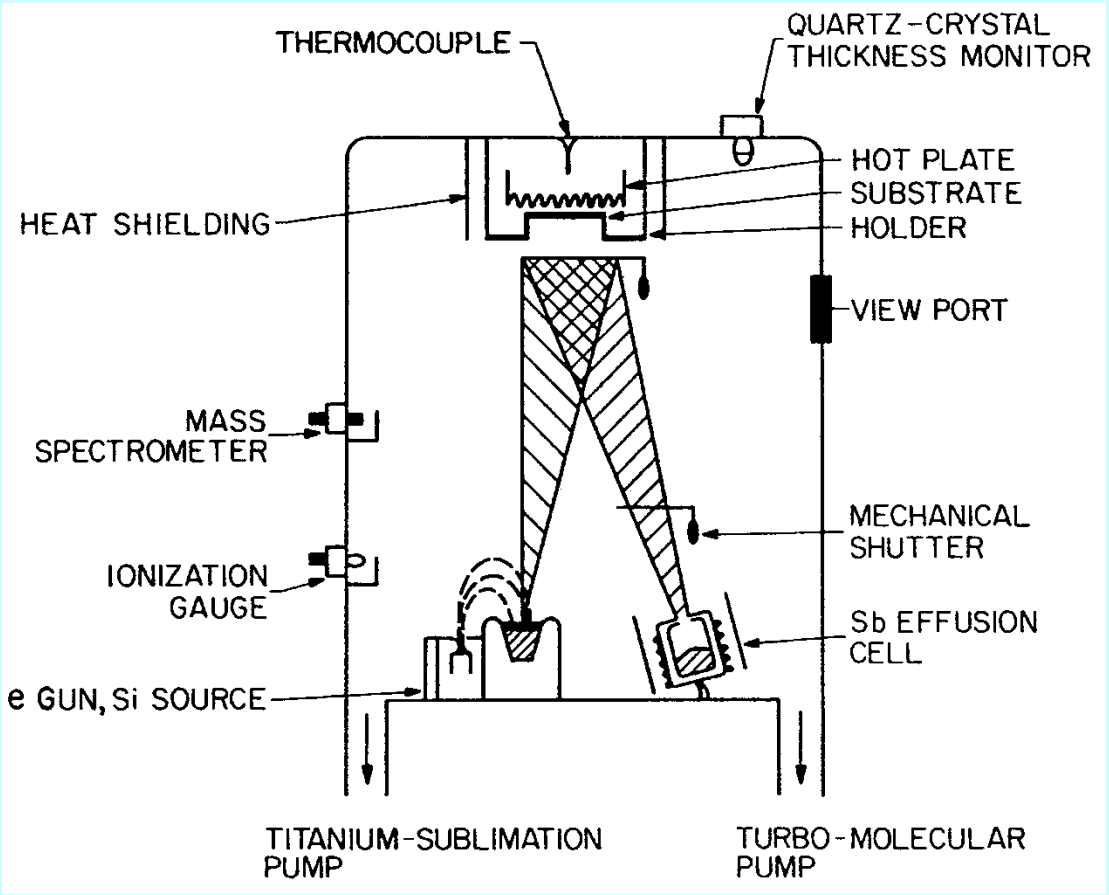
SEG is usually accomplished at reduced partial pressure of the reactant in order to suppress the nucleation of silicon on the dielectric film, thereby resulting in nucleation only on the exposed silicon surface

Low Temperature Epitaxy (LTE)

Low-temperature epitaxy (LTE) of Si produces epitaxial growth at temperature of 550^{o}C or less, much lower than that in conventional epitaxial processes. A low temperature is required to minimize thermal diffusion and mass-transport-controlled processes.

CVD and molecular beam epitaxy (MBE) are the most popular methods. The success of these techniques relies on both an ultra-clean growth environment and a unique Si surface-cleaning process.

Molecular Beam Epitaxy (MBE)



Molecular beam epitaxy, which utilizes evaporation, is a non-CVD epitaxial growth process. MBE is therefore not complicated by boundary-layer transport effects, nor are there chemical reactions to consider. The essence of the process is evaporation of silicon and one or more dopants.

- Silicon MBE is performed under ultra-high vacuum (UHV) conditions of 10^{-8} to 10^{-10} Torr, where the mean free path of the atom is given by $\mathbf{5x10^{-3}/P}$ where $\boldsymbol{P}$ is the system pressure in Torr. At a typical pressure of 10^{-9} Torr, $\boldsymbol{L}$ is $5x10^{6}$ cm, transport velocity is dominated by thermal energy effects

- Lack of intermediate reactions and diffusion effects, coupled with relatively high thermal velocities, results in film properties changing rapidly with any change of the source

- Typical growth temperature is between 400^{o}C and 800^{o}C in order to reduce out-diffusion and autodoping. Growth rates are in the range of 0.01 to 0.3 μm/minute

- Despite the slow growth rate and relatively expensive instrumentation, MBE offers several advantages over conventional CVD for VLSI

- MBE is a low-temperature process that minimizes dopant diffusion and autodoping

- MBE allows more precise control of doping and layer thickness, because CVD is limited by reactant introduction and pumping time constants

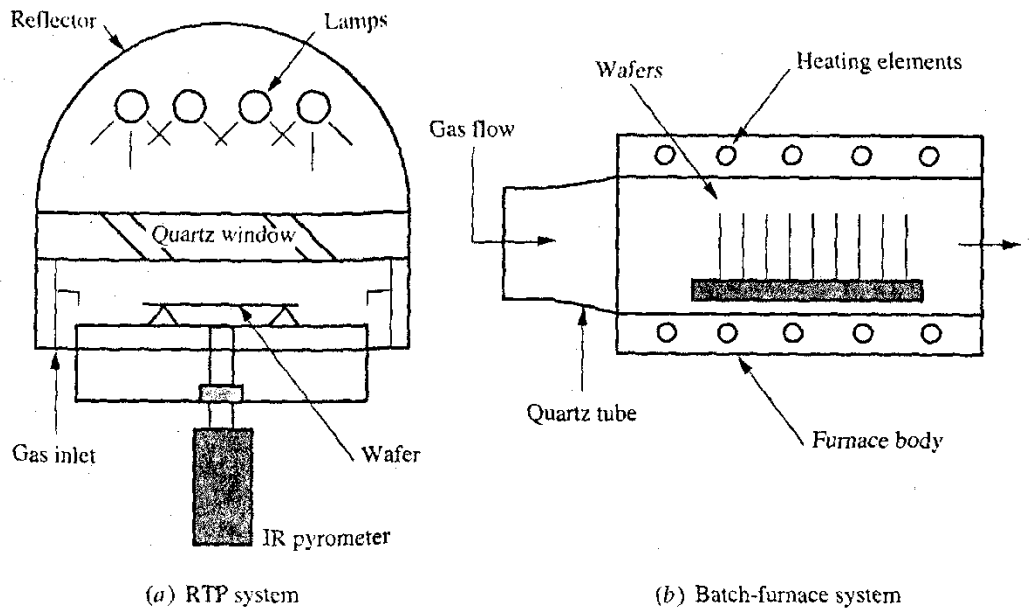
- These advantages are not exploited extensively in silicon IC technology, but MBE has found tremendous usages in microwave and photonic devices made of III-V semiconductors

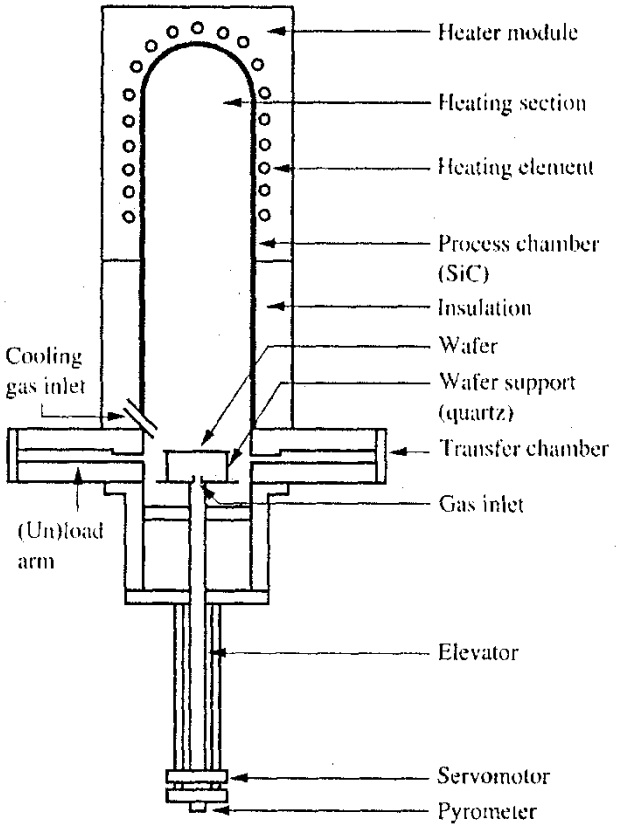
Rapid Thermal Processing (RTP)

- Chemical and physical processes applied to silicon wafers are generally thermally activated. Typical silicon-based processes use batch furnaces for thermal fabrication steps, where a batch consists of 20 to 100 wafers that are simultaneously processed in a single system

- Processing of wafers requires tight control of contamination, process parameters, and reduced manufacturing costs, and some producers are now using single-wafer processing in some steps

- Using transient lamp heating or a continuous heat source (vertical furnace), a single wafer can be heated very quickly to reduce the thermal cycle and mitigate undesirable effects such as dopant diffusion





Rapid thermal processing (RTP) system that is optically heated

Conventional batch-furnace that is resistively heated

Continuous heat source, vertical furnace RTP system

- The most important feature of a rapid thermal annealing processing system consisting of tungsten-halogen lamps is its generation and quick delivery of radiant energy to the wafer (large dT/dt) in a wavelength band of 0.3 to 4.0 μm

- Because of the optical character and wavelength of the energy transfer, the quartz walls do not absorb light efficiently, whereas the silicon wafer does

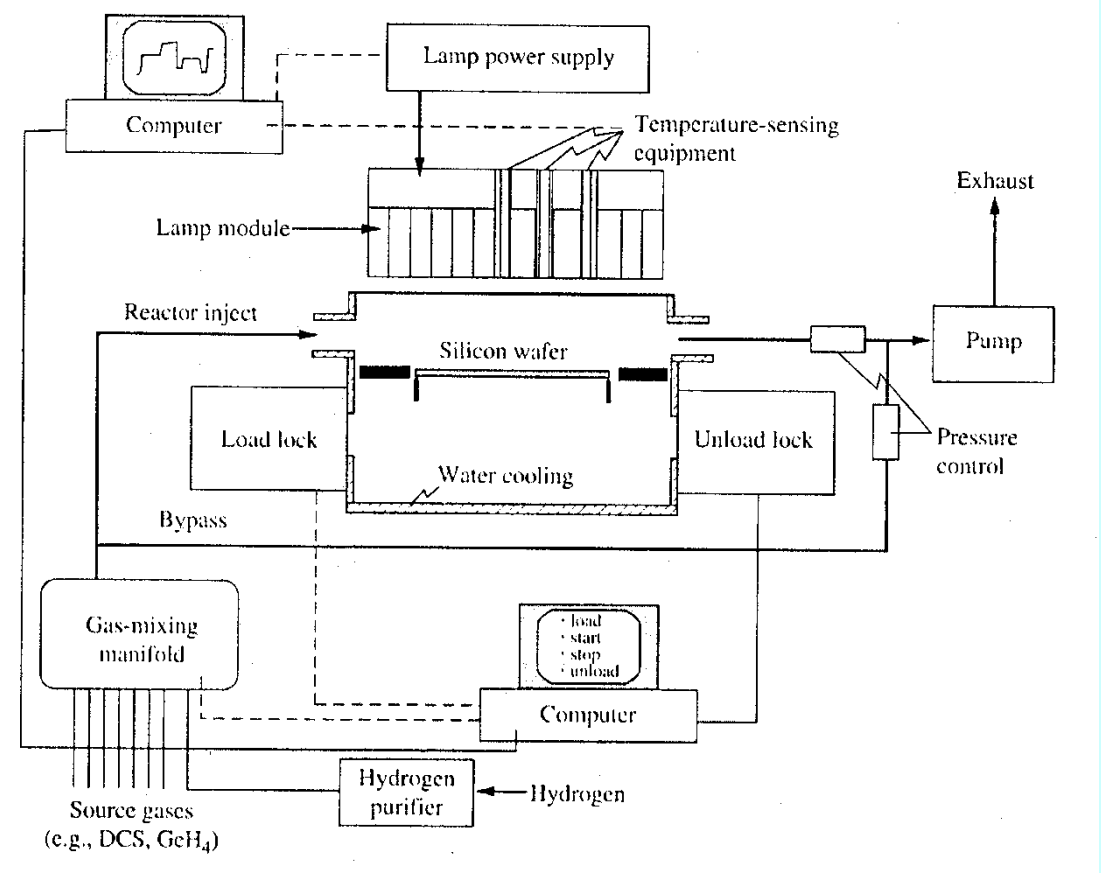
- The wafer is not in thermal equilibrium with the cold walls of the system, allowing for short processing times (seconds to minutes) compared to minutes to hours for conventional furnaces. The reduction in temperature-time exposure afforded by RTP is dramatic

- Rapid heating with large temperature gradients can cause wafer damage in the form of slip dislocations induced by thermal stress and heating can be laterally non-uniform across the wafer

- Conventional furnace processes bring with them significant problems such as particle generation from the hot walls, limited ambient control in an open system, and a large thermal mass that restricts controlled heating time to tens of minutes

- Requirements on contamination, process control, cost, and space are driving a paradigm shift to RTP

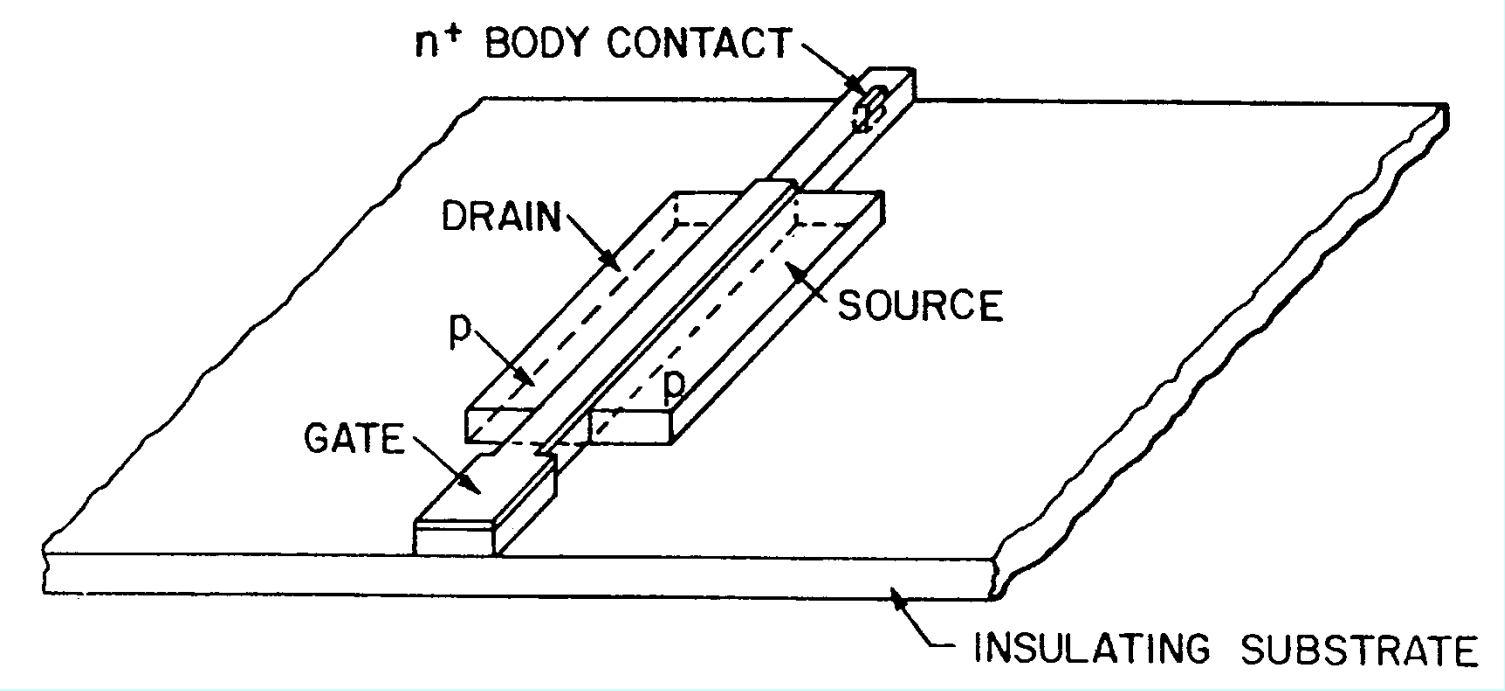
RTP demands on the growth of high-purity epitaxial Si include ambient purity (oxygen and water concentrations in the parts per billion range), optimization of gas flow patterns, minimum wall deposition, and vacuum compatibility.



The deposition process comprises a mass-transport process with a weak temperature dependence and a sequential surface-reaction process that is exponentially dependent on wafer temperature.

Silicon-on-Insulator (SOI)

Silicon device structures have inherent problems that are associated with parasitic circuit elements arising from junction capacitance. These effects become more severe as device dimensions shrink. A viable means to circumvent the problem is to fabricate devices in small islands of silicon on an insulating substrate.



SOI Fabrication Techniques

- Traditional approach is to fabricate such a structure in a silicon epitaxial thin film grown on sapphire (Al_2O_3)

- The lattice parameters of silicon and sapphire are quite similar, high quality SOS (silicon-on-sapphire) epitaxial layers can be fabricated

- The high cost of sapphire substrates, low yield, and lack of commercially viable applications limit the use of SOS to primarily military applications

- SIMOX (separation by implantation of oxygen) utilizes high dose blanket oxygen ion implantation to form a sandwiched buried oxide layer to isolate devices from the wafer substrate

- Wafer bonding utilizes Van der Waals forces to bond two polished silicon wafers, at least one of which is covered with thermal oxide, in a very clean environment at about 1000^{o}C. Mechanical or electrochemical thinning has achieved 1 μm thickness with 0.1 μm deviations

- More recent approaches include the combination of wafer bonding and layer cleavage using hydrogen or helium ion implantation (ion-cut) as well as epitaxial growth on porous silicon and wafer bonding