Chapter 2

Crystal Growth and Wafer Preparation

Professor Paul K. Chu

Advantages of Si over Ge

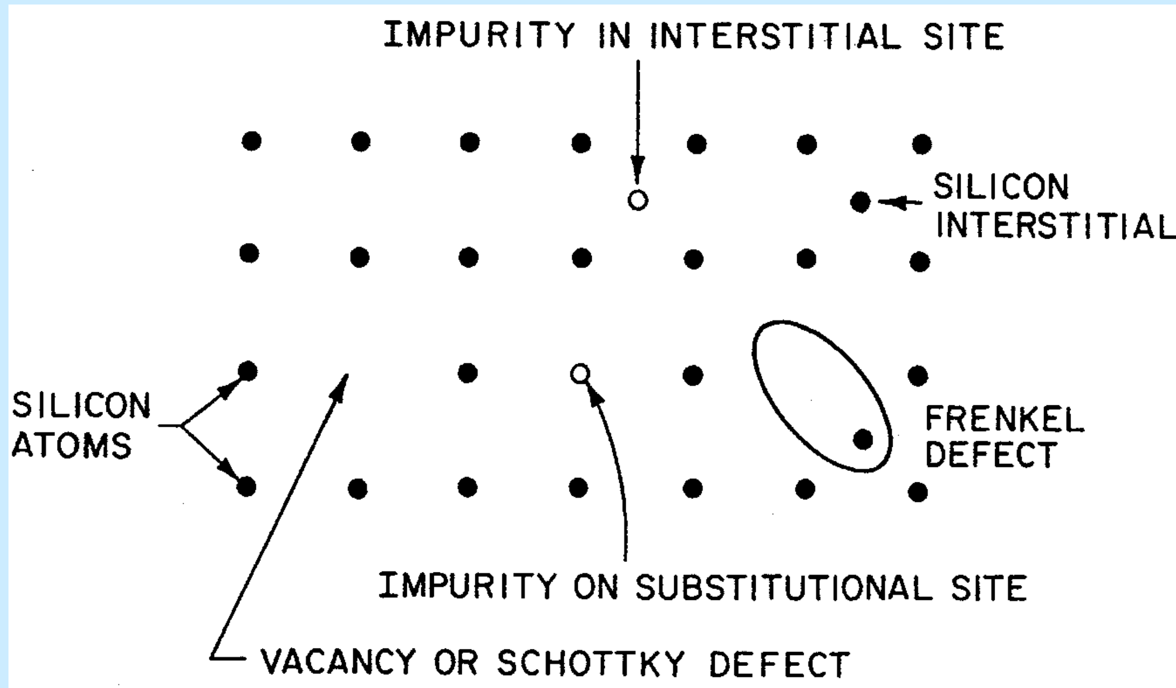
- Si has a larger bandgap (1.1 eV for Si versus 0.66 eV for Ge)
- Si devices can operate at a higher temperature (150^oC vs 100^oC)
- Intrinsic resistivity is higher (2.3×10^5 Ω-cm vs 47 Ω-cm)
- SiO_2 is more stable than GeO_2 which is also water soluble
- Si is less costly

The processing characteristics and some material properties of silicon wafers depend on its orientation.

The <111> planes have the highest density of atoms on the surface, so crystals grow most easily on these planes and oxidation occurs at a higher pace when compared to other crystal planes.

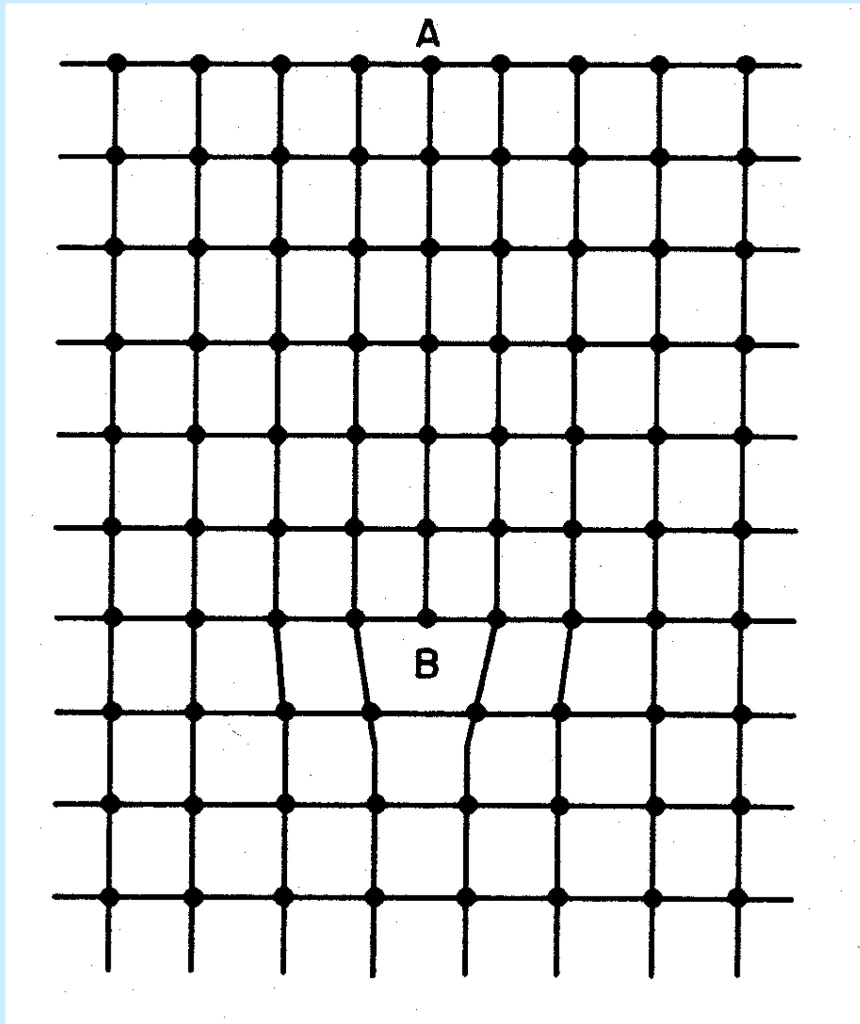
Traditionally, bipolar devices are fabricated in <111> oriented crystals whereas <100> materials are preferred for MOS devices.

Defects



Any non-silicon atoms incorporated into the lattice at either a substitutional or interstitial site are considered point defects

Point defects are important in the kinetics of diffusion and oxidation. Moreover, to be electrically active, dopants must occupy substitutional sites in order to introduce an energy level in the bandgap.

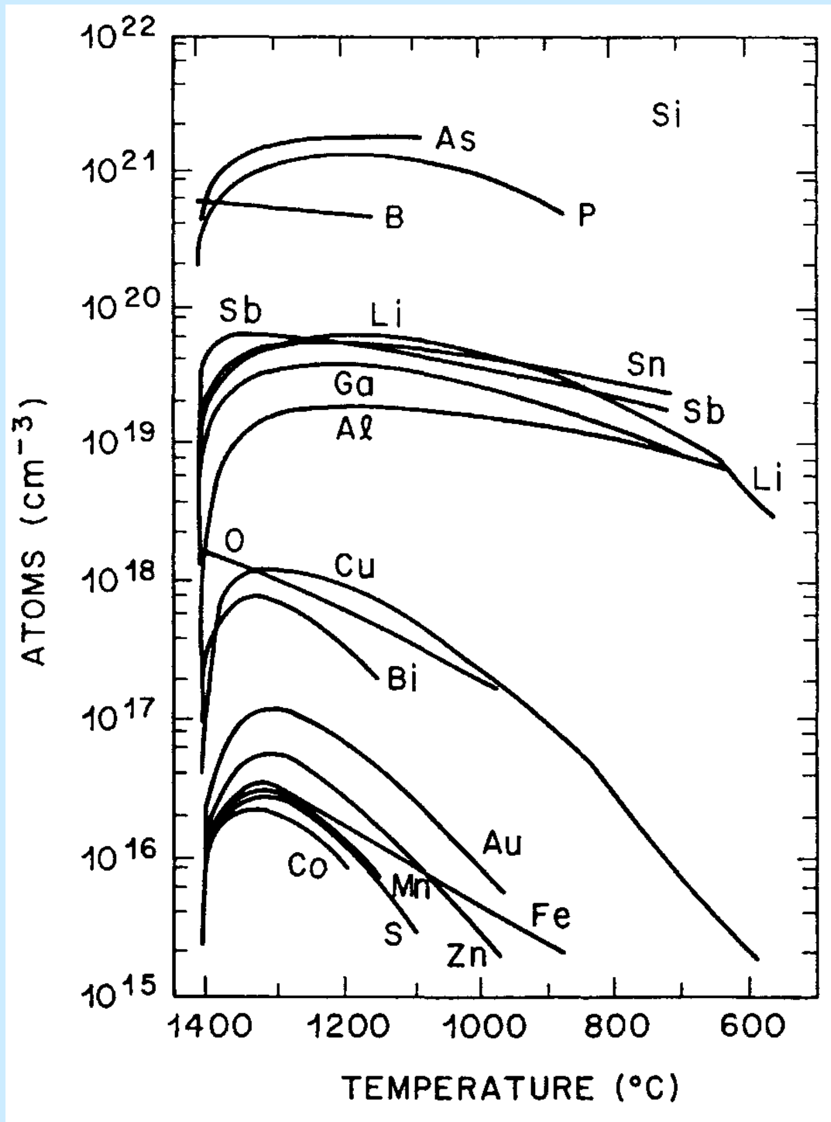


Dislocations are line defects. Dislocations in a lattice are dynamic defects. That is, they can diffuse under applied stress, dissociate into two or more dislocations, or combine with other dislocations.

Dislocations in devices are generally undesirable, because they act as sinks for metallic impurities and alter diffusion profiles.

Defects

- Two typical area or planar defects are twins and grain boundaries
- Twinning represents a change in the crystal orientation across a twin plane, such that a mirror image exists across that plane
- Grain boundaries are more disordered than twins and separate grains of single crystals in polycrystalline silicon
- Planar defects appear during crystal growth, and crystals having such defects are not considered usable for IC manufacture and are discarded



Precipitates of impurity or dopant atoms constitute the fourth class of defects. The solubility of dopants varies with temperature, and so if an impurity is introduced at the maximum concentration allowed by its solubility, a supersaturated condition will exist upon cooling. The crystal achieves an equilibrium state by precipitating the impurity atoms in excess of the solubility level as a second phase.

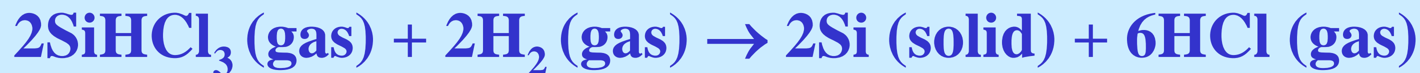
Precipitates are generally undesirable as they act as sites for dislocation generation. Dislocations result from the volume mismatch between the precipitate and the lattice, inducing a strain that is relieved by the formation of dislocations.

Electronic Grade Silicon

Electronic-grade silicon (EGS), a polycrystalline material of high purity, is the starting material for the preparation of single crystal silicon. EGS is made from metallurgical-grade silicon (MGS) which in turn is made from quartzite, which is a relatively pure form of sand. MGS is purified by the following reaction:

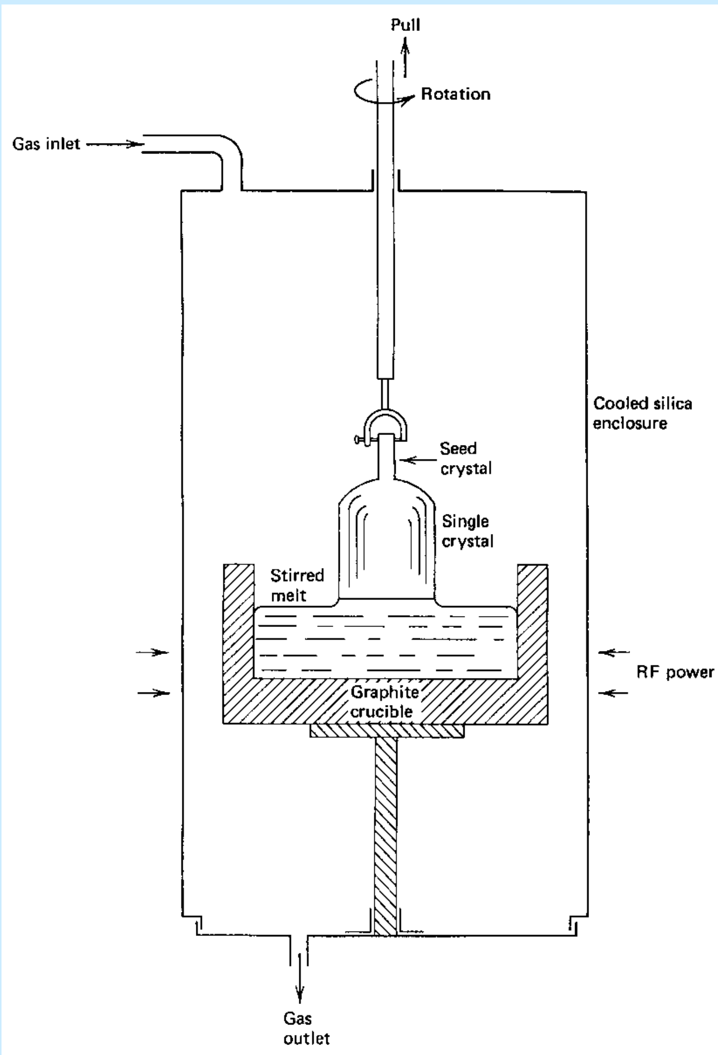
$$\mathrm{Si\ (solid) + 3HCl\ (gas) \rightarrow SiHCl_3\ (gas) + H_2\ (gas) + heat}$$

The boiling point of trichlorosilane ($SiHCl_3$) is 32°C and can be readily purified using fractional distillation. EGS is formed by reacting trichlorosilane with hydrogen:



$$\mathrm{2SiHCl_3\ (gas) + 2H_2\ (gas) \rightarrow 2Si\ (solid) + 6HCl\ (gas)}$$

Czochralski Crystal Growth



The Czochralski (CZ) process, which accounts for 80% to 90% of worldwide silicon consumption, consists of dipping a small single-crystal seed into molten silicon and slowly withdrawing the seed while rotating it simultaneously.

The crucible is usually made of quartz or graphite with a fused silica lining. After the seed is dipped into the EGS melt, the crystal is pulled at a rate that minimizes defects and yields a constant ingot diameter.

Impurity Segregation

Impurities, both intentional and unintentional, are introduced into the silicon ingot. Intentional dopants are mixed into the melt during crystal growth, while unintentional impurities originate from the crucible, ambient, etc.

All common impurities have different solubilities in the solid and in the melt. An equilibrium segregation coefficient k_o can be defined to be the ratio of the equilibrium concentration of the impurity in the solid to that in the liquid at the interface, i.e. $k_o = C_s/C_l$. **Note that all the values shown in the table are below unity, implying that the impurities preferentially segregate to the melt and the melt becomes progressively enriched with these impurities as the crystal is being pulled.**

Impurity	Al	As	B	C	Cu	Fe	O	P	Sb
k_o	0.002	0.3	0.8	0.07	4×10^{-6}	8×10^{-6}	0.25	0.35	0.023

Impurity Distribution

The distribution of an impurity in the grown crystal can be described mathematically by the normal freezing relation:

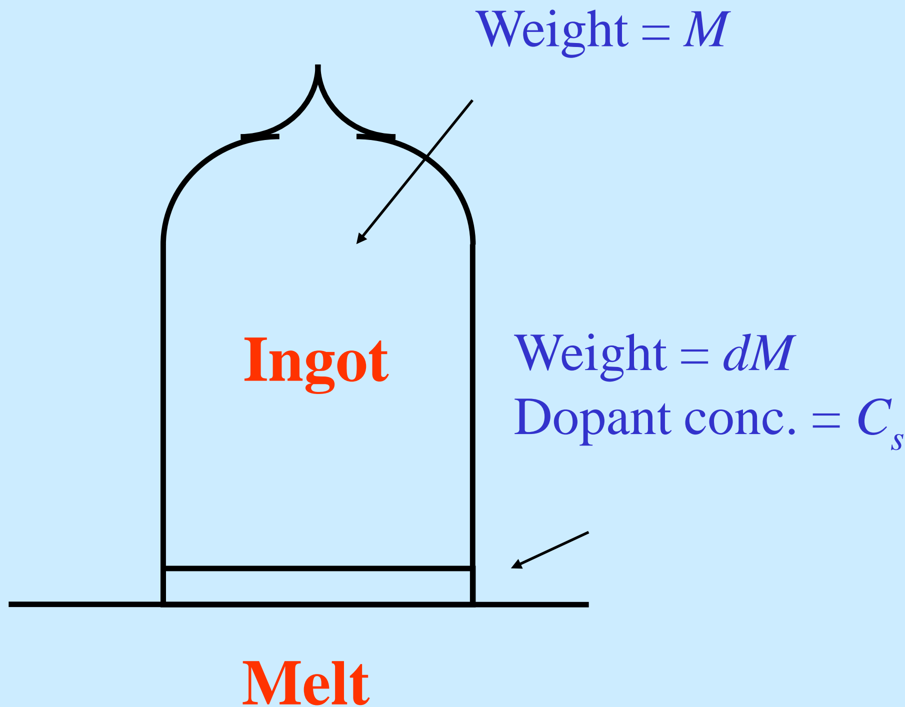
$$C_s = k_o C_o (1 - X)^{k_o - 1}$$

***X* is the fraction of the melt solidified**

C_o is the initial melt concentration

C_s is the solid concentration

k_o is the segregation coefficient



Consider a crystal being grown from a melt having an initial weight M_o with an initial dopant concentration C_o in the melt (i.e., the weight of the dopant per 1 gram melt).

At a given point of growth when a crystal of weight M has been grown, the amount of the dopant remaining in the melt (by weight) is S.

For an incremental amount of the crystal with weight dM, the corresponding reduction of the dopant ($-dS$) from the melt is $C_s\ dM$, where C_s is the dopant concentration in the crystal (by weight): $-dS = C_s\ dM$

The remaining weight of the melt is M_o **-** M, and the dopant concentration in the liquid (by weight), C_l, is given by $C_l = \frac{S}{M_o - M}$

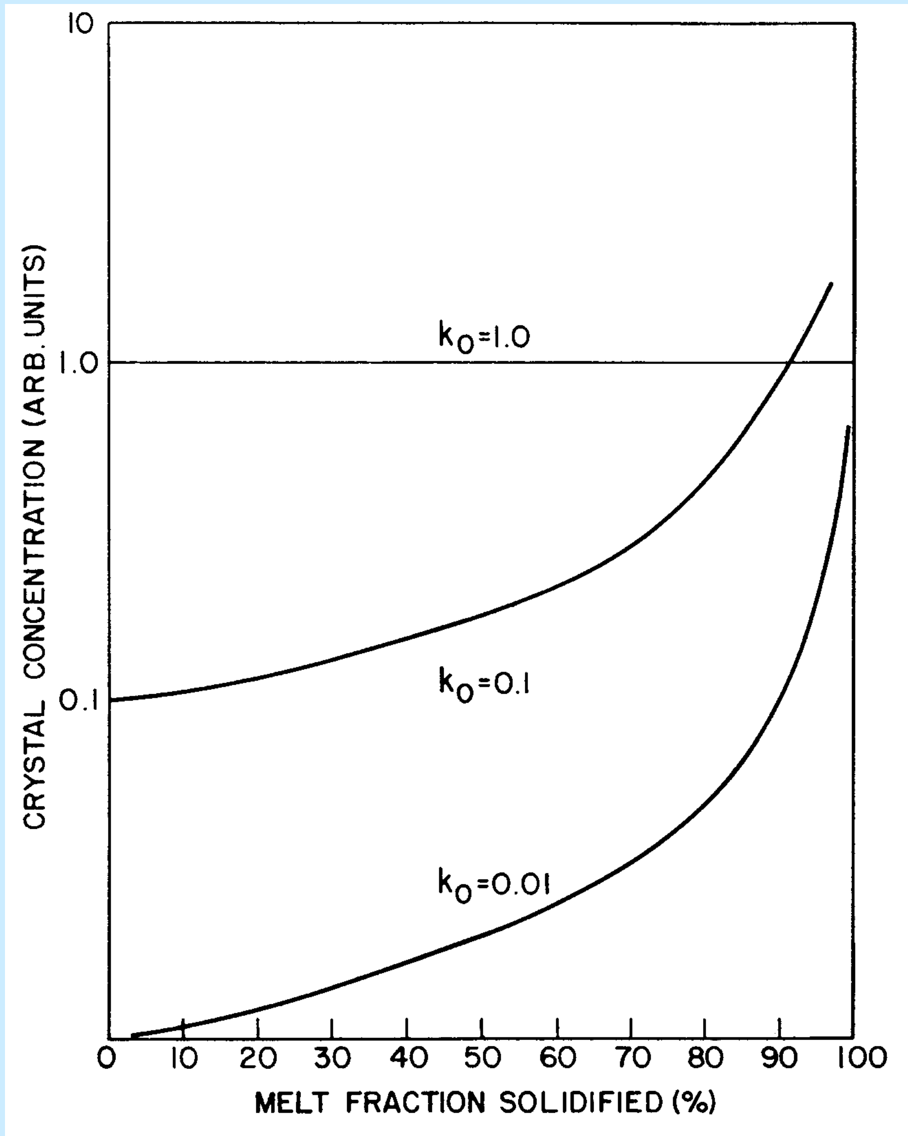
Combining the two equations and substituting $C_s / C_l = k_o$

$$\frac{dS}{S} = -k_o \left[\frac{dM}{M_o - M} \right]$$

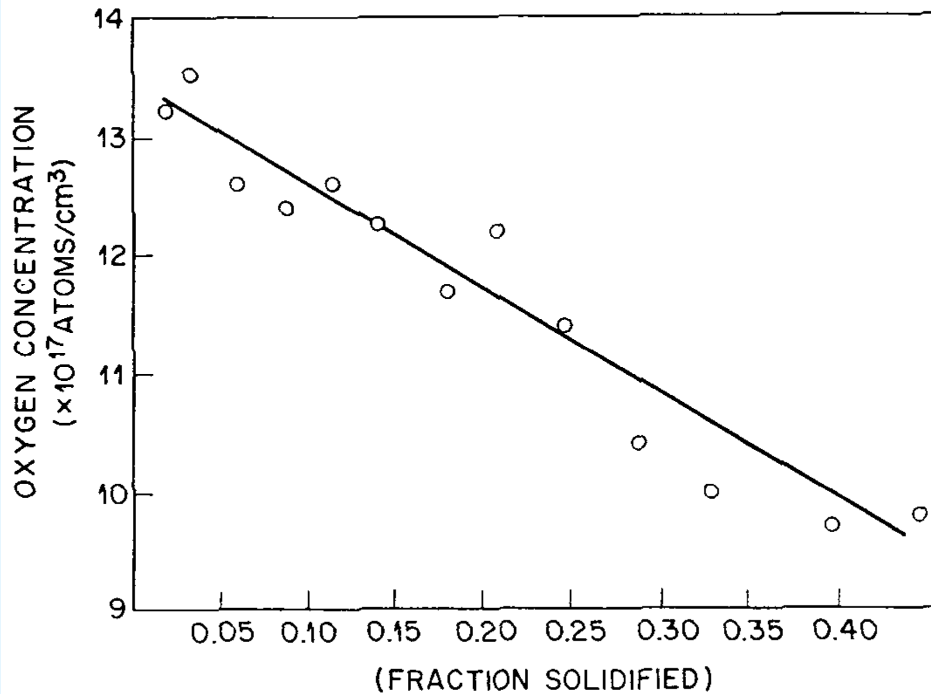
Given the initial weight of the dopant, $C_o M_o$, we can integrate and obtain

$$\int_{C_o M_o}^{S} \frac{dS}{S} = k_o \int_{o}^{M} \frac{-dM}{M_o - M}$$

Solving the equation gives $C_s = k_o C_o \left[1 - \frac{M}{M_o} \right]^{k_o - 1}$



Impurity concentration profiles along the silicon ingot (axially) for different k_o with $C_o = 1$



CZ-Si crystals are grown from a silicon melt contained in a fused silica (SiO_2) crucible. Fused silica reacts with hot silicon and releases oxygen into the melt giving CZ-Si an indigenous oxygen concentration of about 10^{18} atoms/cm^3.

Although the segregation coefficient of oxygen is <1, the axial distribution of oxygen is governed by the amount of oxygen in the melt. Less dissolution of the crucible material occurs as the melt volume diminishes, and less oxygen is available for incorporation.

Oxygen in Silicon

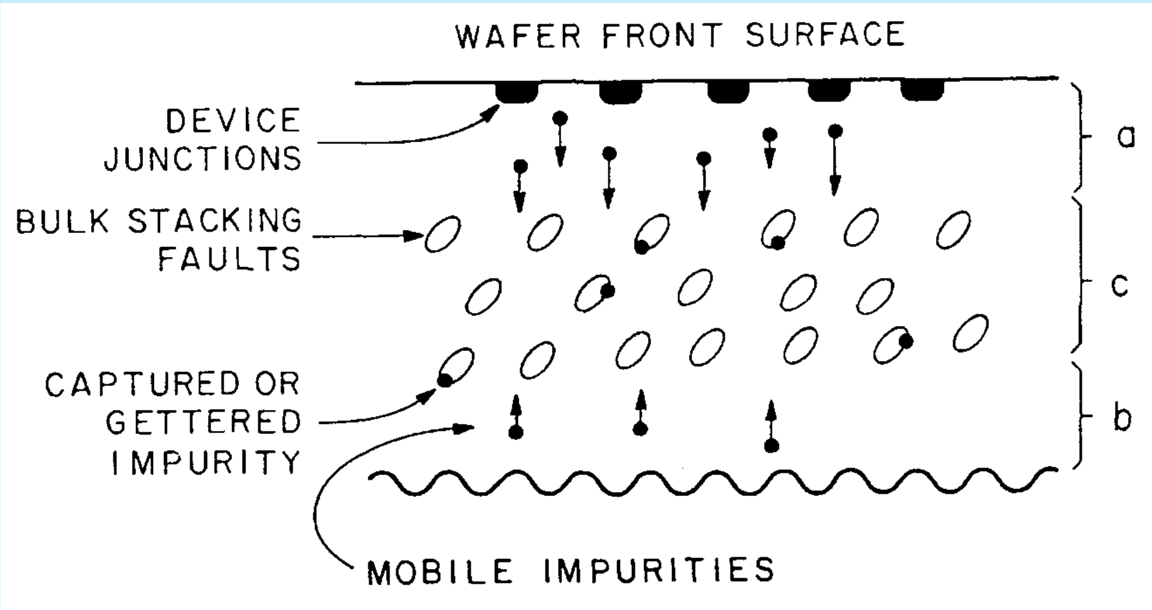
- Oxygen forms a thermal donor in silicon
- Oxygen increases the mechanical strength of silicon
- Oxygen precipitates provide gettering sites for unintentional impurities

Thermal Donors

- Thermal donors are formed by the polymerization of Si and O into complexes such as SiO_4 in interstitial sites at 400^oC to 500^oC

- Careful quenching of the crystal annihilates these donors

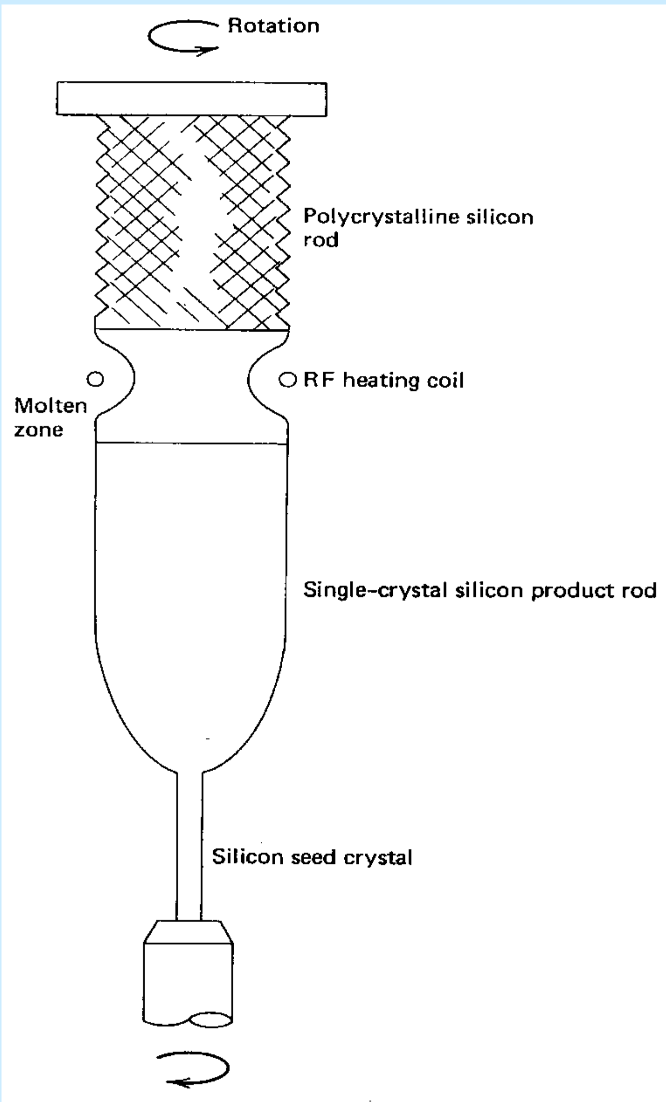
Internal Gettering



Under certain annealing cycles, oxygen atoms in the bulk of the crystal can be precipitated as SiO_x clusters that act as trapping sites to impurities.

This process is called internal gettering and is one of the most effective means to remove unintentional impurities from the near surface region where devices are fabricated.

Float-Zone Process



The float-zone process has some advantages over the Czochralski process for the growth of certain types of silicon crystals.

The molten silicon in the float-zone apparatus is not contained in a crucible, and is thus not subject to the oxygen contamination present in CZ-Si crystals.

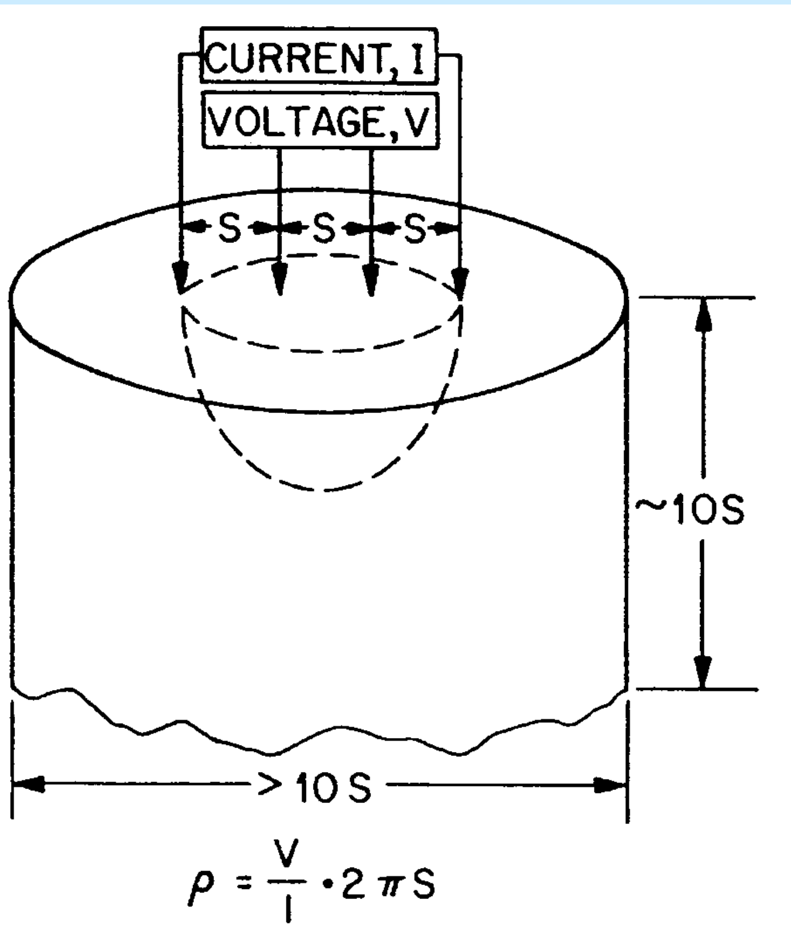
The float-zone process is also necessary to obtain crystals with a high resistivity (>> 25 W-cm).

Characterization

- Routine evaluation of ingots or boules involves measuring the resistivity, evaluating their crystal perfection, and examining their mechanical properties, such as size and mass

- Other tests include the measurement of carbon, oxygen, and heavy metals

Resistivity Measurement

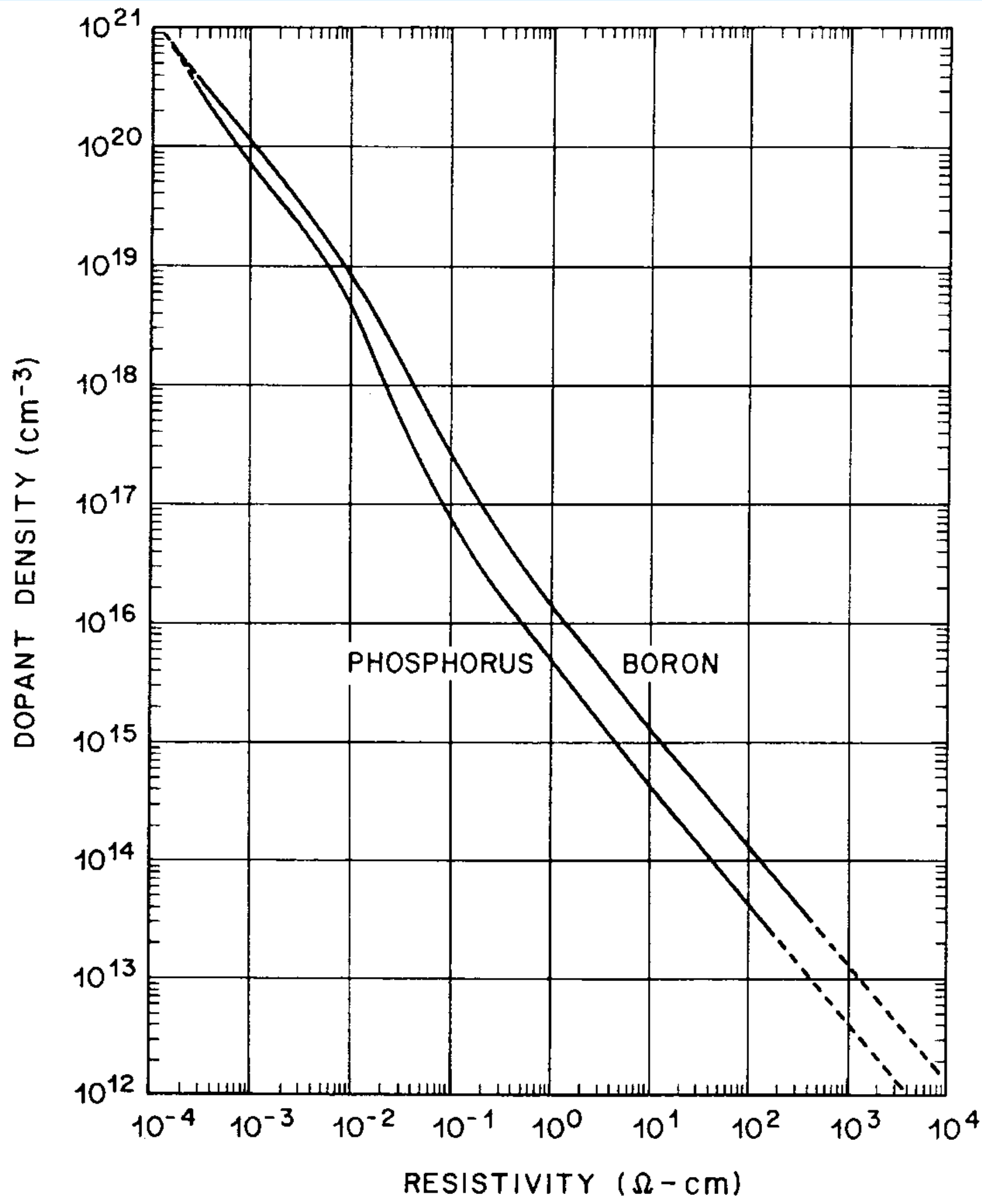


Resistivity measurements are made on the flat ends of the crystal by the **four-point probe** technique.

A current, ***I***, is passed through the outer probes and the voltage, ***V***, is measured between the inner probes.

The measured resistance (***V***/***I***) is converted to resistivity (W-cm) using the relationship:

$$\rho = (V/I)2\pi S$$



The calculated resistivity can be correlated with dopant concentration using a dopant concentration versus resisitivity chart

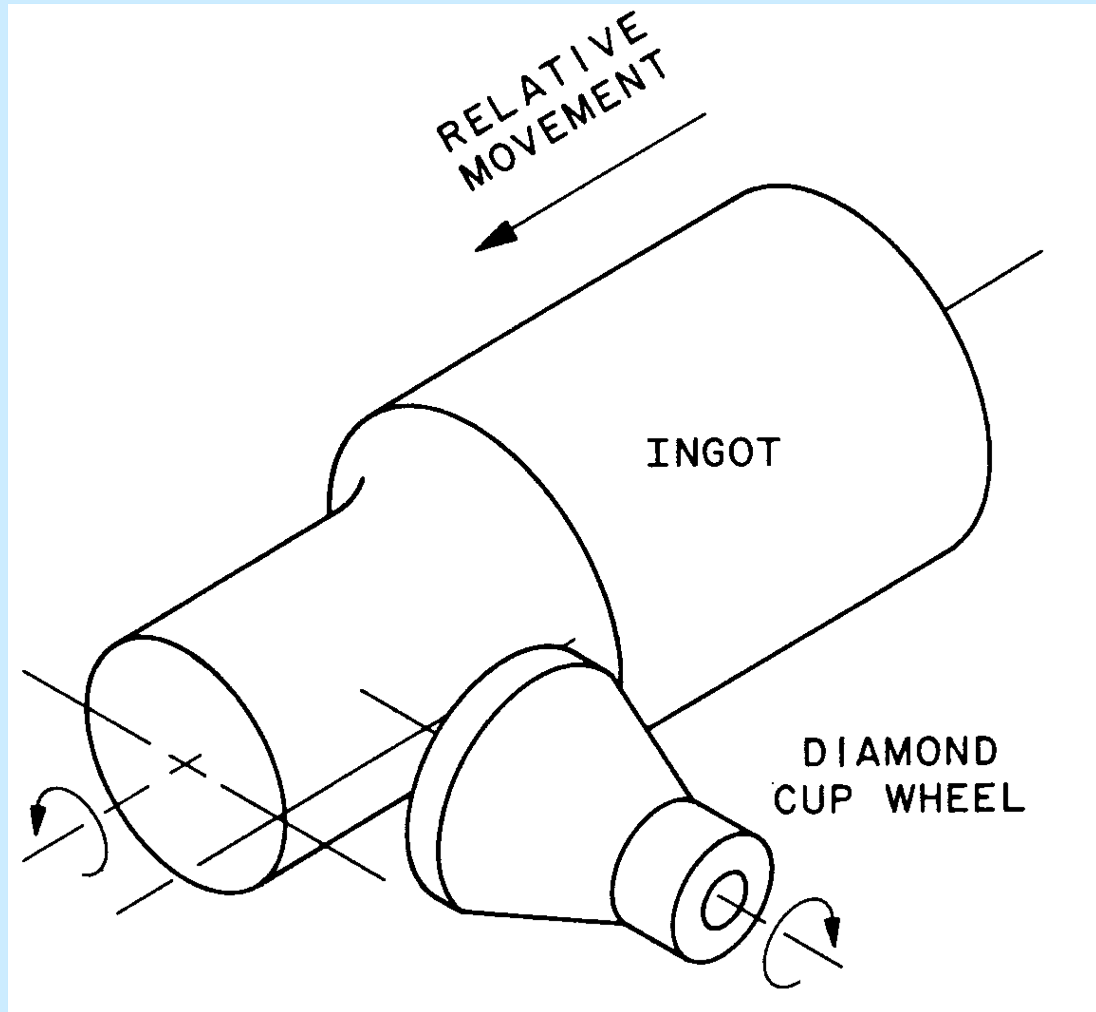
Wafer Preparation

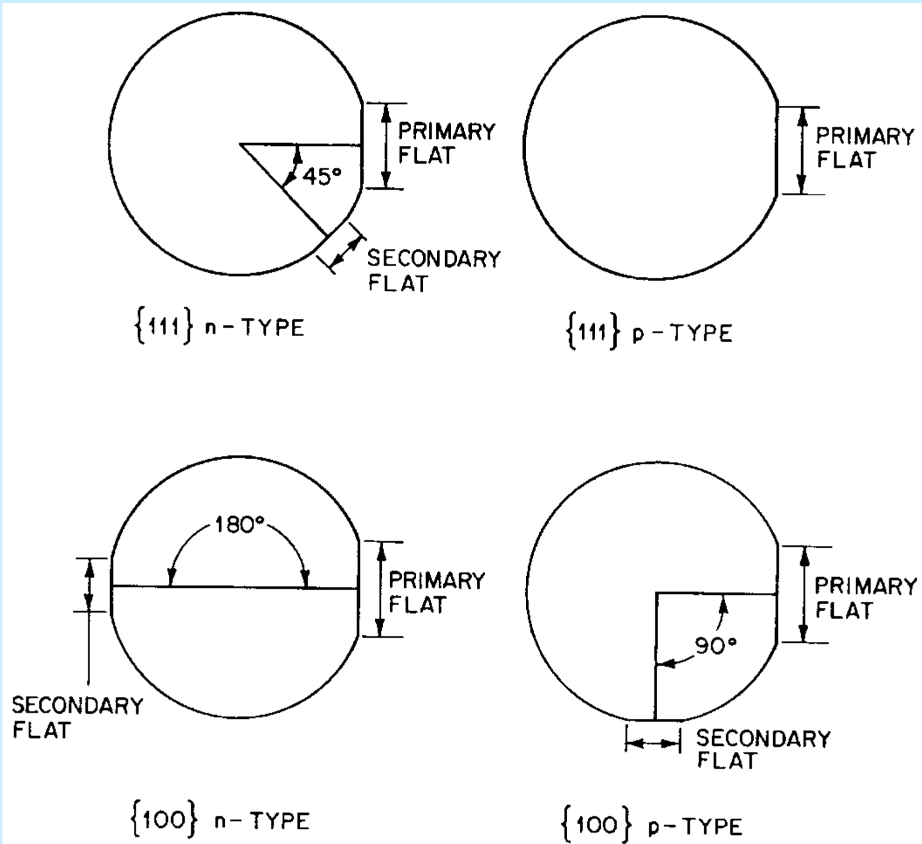
- Gross crystalline imperfections are detected visually and defective crystals are cut from the boule. More subtle defects such as dislocations can be disclosed by preferential chemical etching

- Chemical information can be acquired employing wet analytical techniques or more sophisticated solid-state and surface analytical methods

- Silicon, albeit brittle, is a hard material. The most suitable material for shaping and cutting silicon is industrial-grade diamond. Conversion of silicon ingots into polished wafers requires several machining, chemical, and polishing operations

Grinding





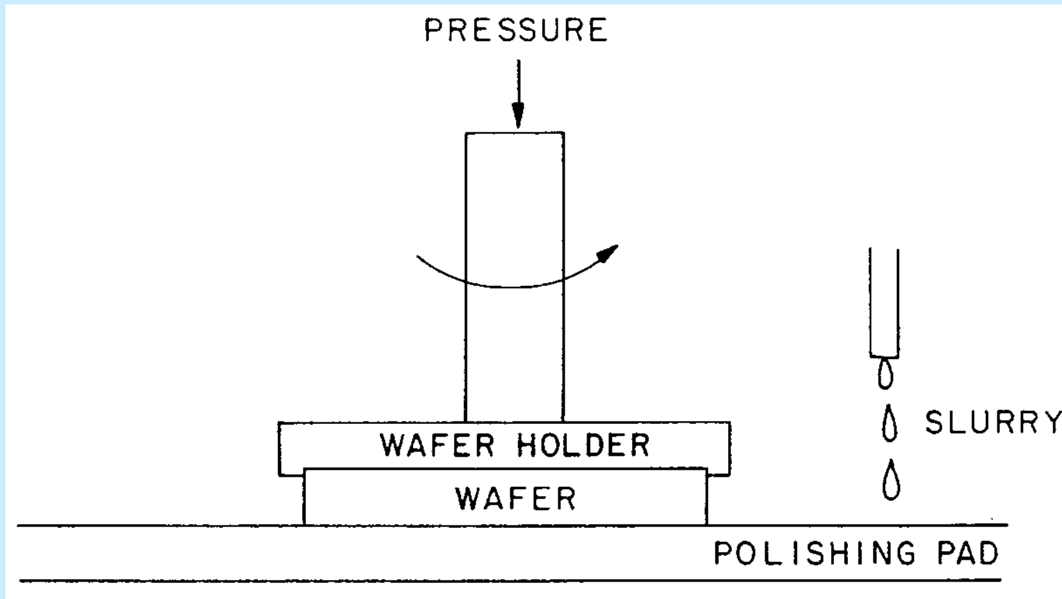
After grinding to fix the diameter, one or more flats are grounded along the length of the ingot. The largest flat, called the "major" or "primary" flat, is usually relative to a specific crystal orientation. The flat is located by x-ray diffraction techniques.

The primary flat serves as a mechanical locator in automated processing equipment to position the wafer, and also serves to orient the IC device relative to the crystal. Other smaller flats are called "secondary" flats that serve to identify the orientation and conductivity type of the wafer.

The drawback of these flats is the reduction of the usable area on the wafer. For some 200 mm and 300 mm diameter wafers, only a small notch is cut from the wafer to enable lithographic alignment but no dopant type or crystal orientation information is conveyed.

Slicing determines four wafer parameters:

- Surface orientation (e.g., <111> or <100>)
- Thickness (e.g., 0.5 – 0.7 mm, depending on wafer diameter)
- Taper, which is the wafer thickness variations from one end to another
- Bow, which is the surface curvature of the wafer measured from the center of the wafer to its edge



Finished Wafers

The wafer as cut varies enough in thickness to warrant an additional lapping operation that is performed under pressure using a mixture of Al_2O_3 and glycerine. Subsequent chemical etching removes any remaining damaged and contaminated regions.

Polishing is the final step. Its purpose is to provide a smooth, specular surface on which device features can be photoengraved.

Typical Specifications for Silicon Wafers

Parameter	**125 mm**	**150 mm**	**200 mm**	**300 mm**
Diameter (mm)	125±1	150±1	200±1	300±1
Thickness (mm)	0.6-0.65	0.65-0.7	0.715-0.735	0.755-0.775
Bow (µm)	70	60	30	<30
Total thickness variation (µm)	65	50	10	<10
Surface orientation	±1°	±1°	±1°	±1°