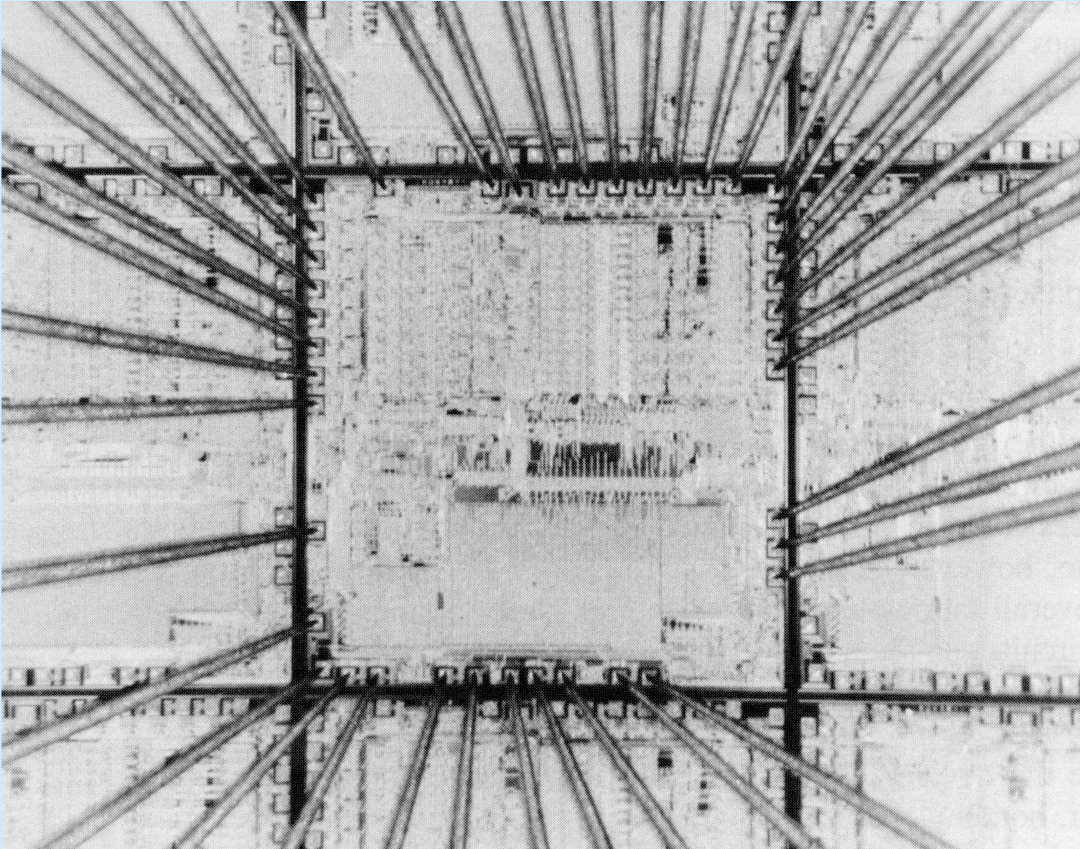
Chapter 11

Testing, Assembly, and Packaging

Professor Paul K. Chu

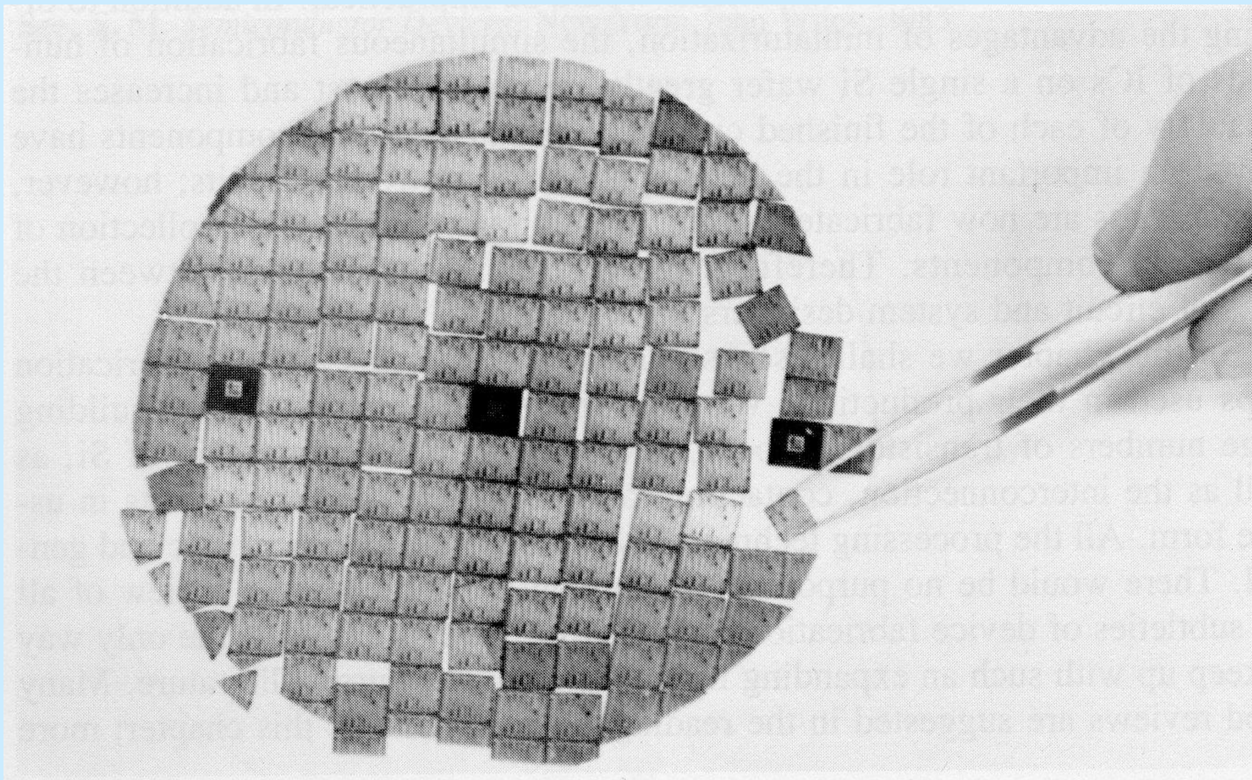
Testing



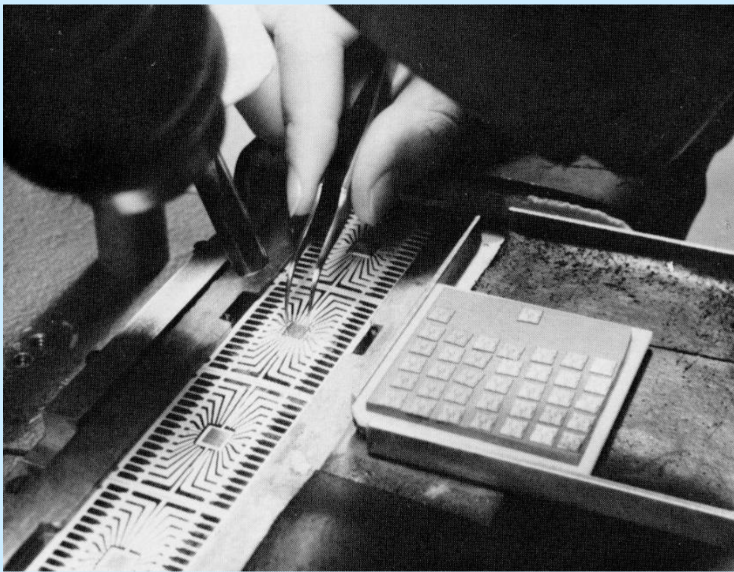
- The finished wafer is put on a holder and aligned for testing under a microscope
- Each chip on the wafer is inspected by a multiple-point probe

- The probe contacts the various pads on an individual circuit and a series of tests are made to examine the electrical properties of the device
- The tests are conducted automatically in a very short time ranging from a few milliseconds for a simple circuit to 30 seconds or more for a complex chip
- The test results are fed into a computer, and a decision is made regarding the acceptability of the circuit
- If the chip is defective or the circuit falls below specifications, the computer instructs the test probe to mark the circuit with a dot of ink
- The probe automatically steps the prescribed distance to the next chip on the wafer and repeats the process

After all of the circuits have been tested and substandard ones marked, the wafer is removed from the testing machine, thinned (150 mm diameter wafers thinned from 650 μm to approximately 400 μm thick), mounted onto an adhesive tape, and scribed using a dicing saw with a diamond blade

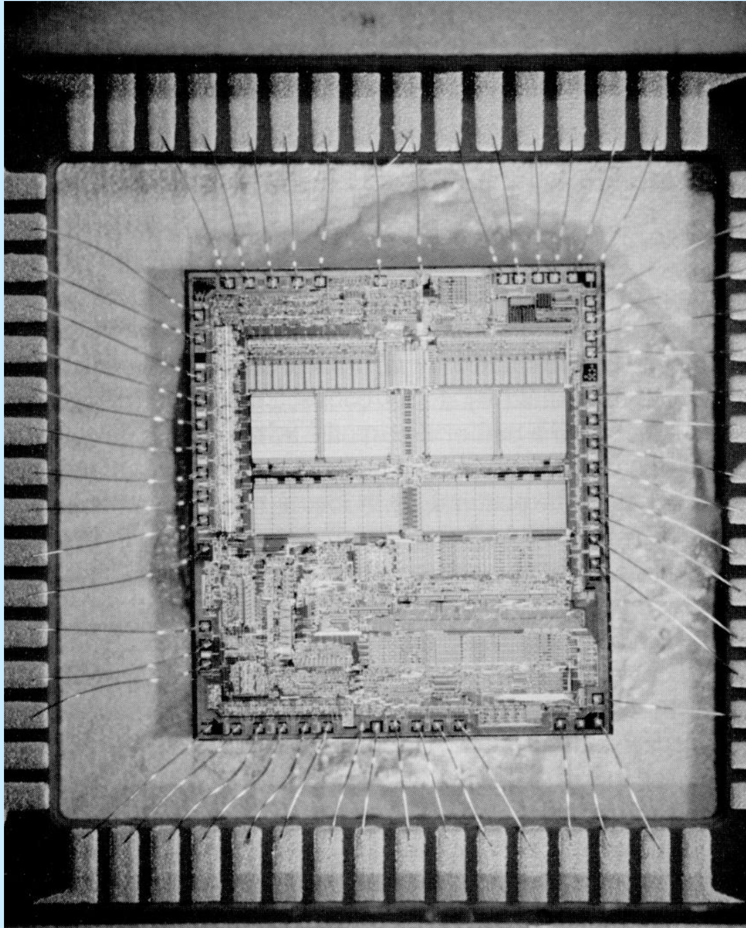


Die Bonding



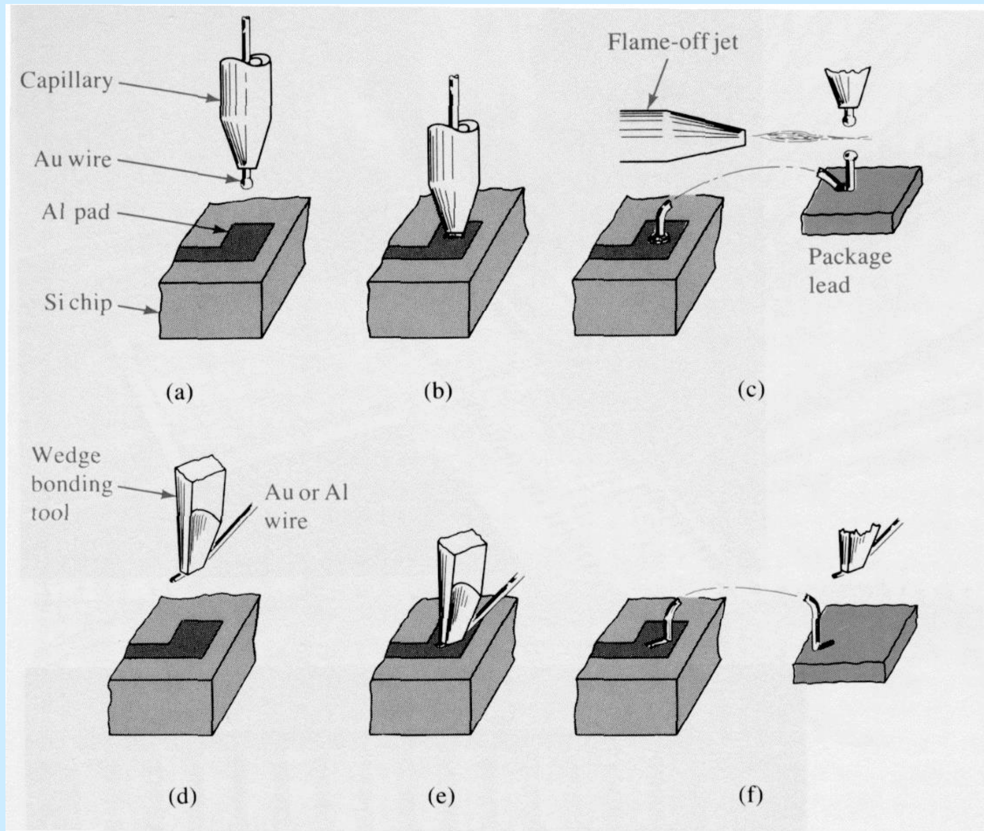
A thin layer of Au (typically combined with Ge or other elements to improve the metallurgical contact) is placed between the bottom of the chip and the lead frame. Heat and a slight scrubbing motion are applied to form an alloyed bond holding the chip firmly to the substrate

Wire Bonding



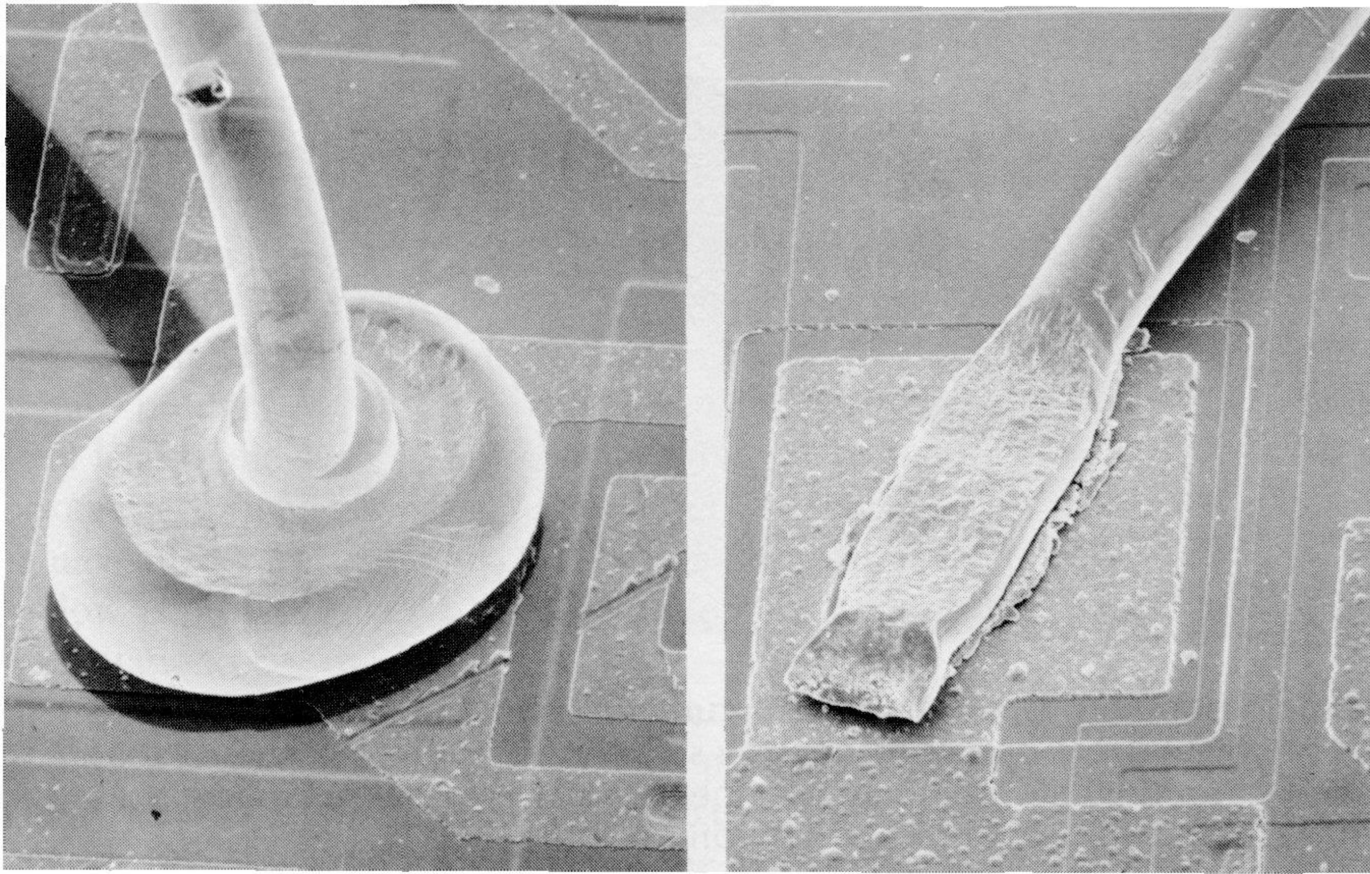
After the chip has been mounted, interconnecting wires are attached from the various contact pads on the IC to the posts on the lead frame

Wire Bonding

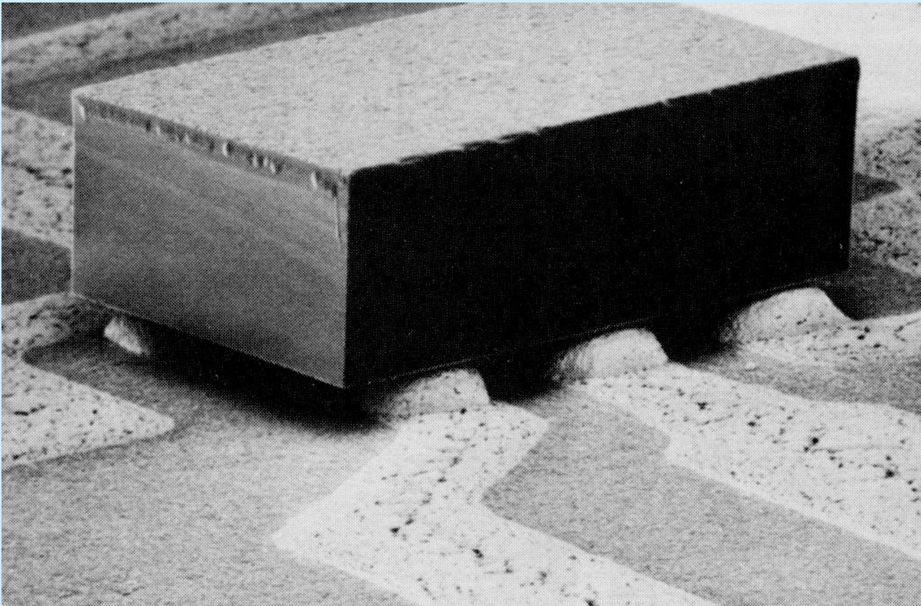


a. Capillary positioned over one of the contact pads for a ball (nail-head) bond
b. Pressure exerted to bond the wire to the pad
c. Post bond and flame-off
d. Wedge bonding tool
e. Pressure, ultrasonic, or thermal energy applied
f. Post bond completed and wire broken or cut from next bond

Ball Bond Wedge Bond



Flip - Chip Technique



- Bumps of solder or special metal alloys rising about 50 μm above the surface of the chip are deposited on each contact pad
- each chip is turned upside down and the bumps are properly aligned with the metallization pattern on the substrate

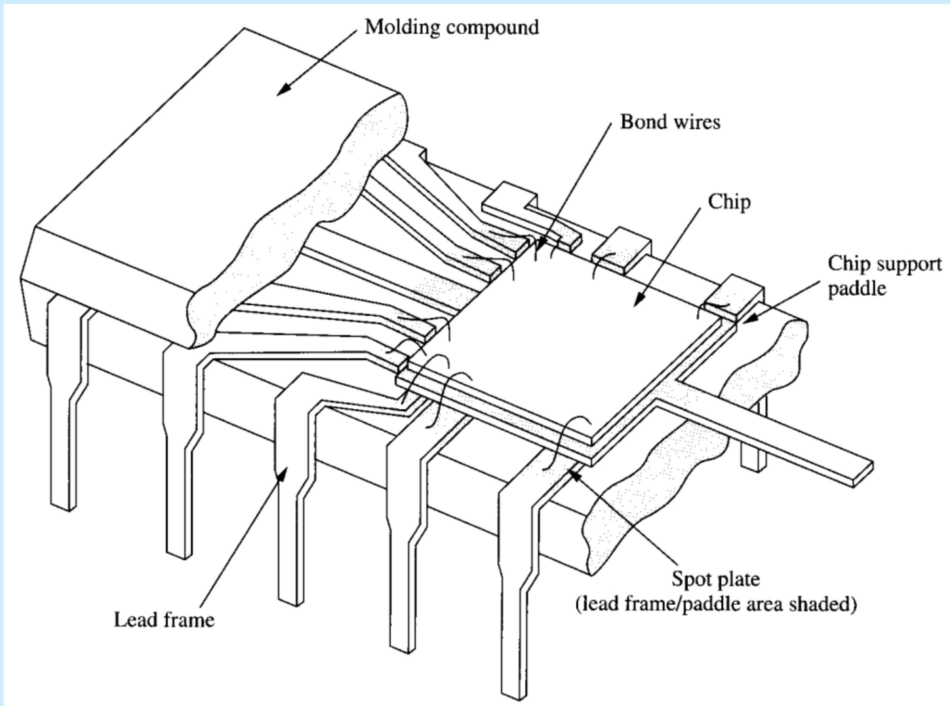
Packaging

- Chips must be contained (packaged) in a suitable medium protecting them from the environment of their intended application
- Some ICs must be isolated from moisture and contaminants thus demanding better packaging techniques
- Bonds and other elements of ICs must be protected from corrosion and mechanical shock

Plastic Package

- Chips encapsulated with resin materials, typically epoxy based resin
- Chips not perfectly isolated from the external environment and outside ambient affects the chip over time and gradually penetrates the plastic
- More economical than hermetic packages

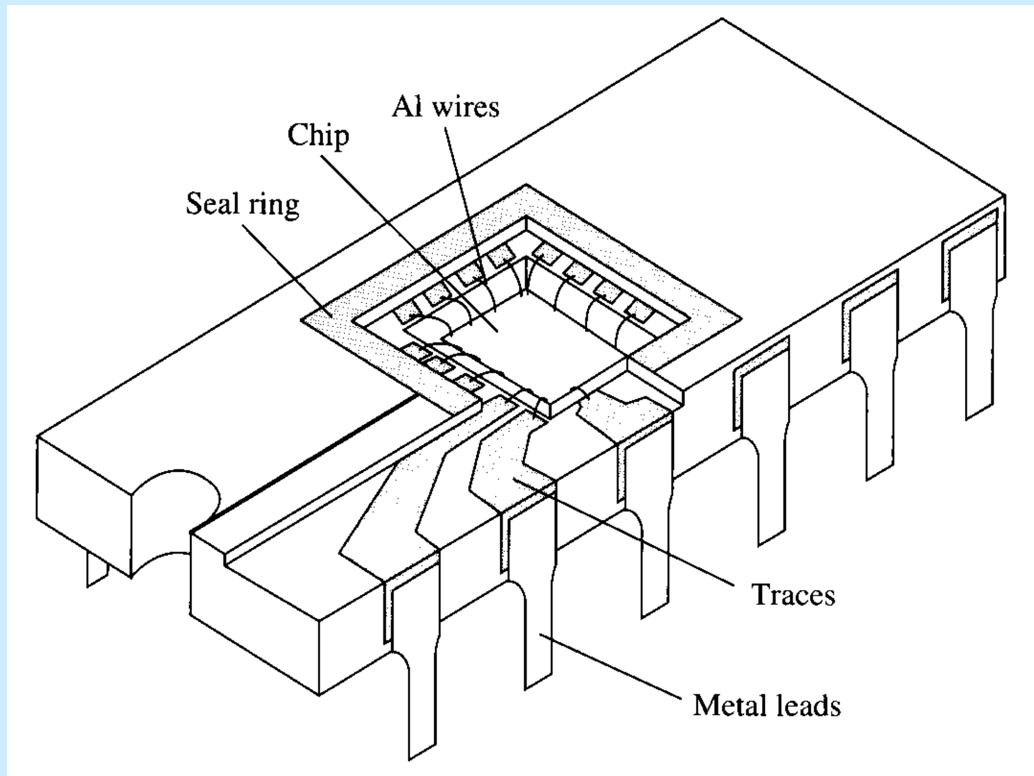
Plastic Package



The package cannot thoroughly decouple the chip from the environment, and so the mechanical and chemical effects from the plastic touching the chip require attention

- The chip is attached to the paddle of the lead frame made of etched or stamped thin metal (usually Fe-Ni or Cu alloys)
- The frame provides external leads in the completed package
- Encapsulation is conducted by molding using epoxy resin that covers the chip and forms the outer shape of the package at the same time
- External leads are formed into the final shape after molding

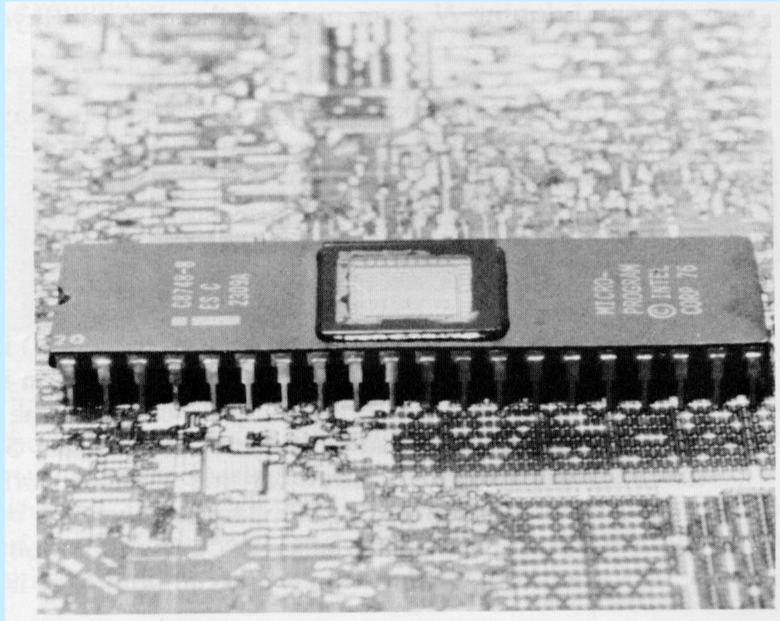
Hermetic Package



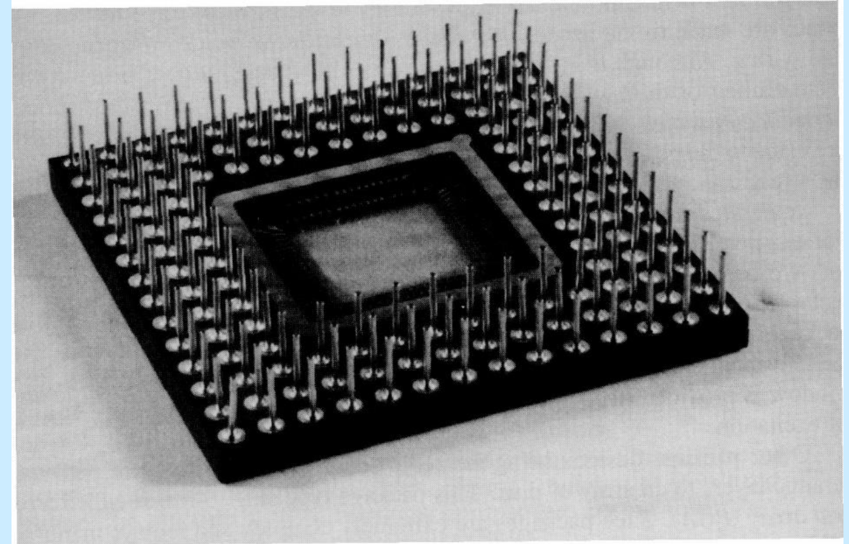
The package excludes environmental contaminants and has little mechanical or chemical effect on the chip, since the package components do not touch the chip surface

- The chip resides in a cavity of a ceramic package
- Hermetic sealing is complete with the cap, usually ceramic or metal, lidded to the package
- Al_2O_3 is the usual ceramic material, and AlN is used when higher power dissipation is required

Through – Hole Package



Dual–in–line package (**DIP**): A transparent lid is included over the chip for erasure of the EPROM (electrically programmable read only memory) by ultraviolet light

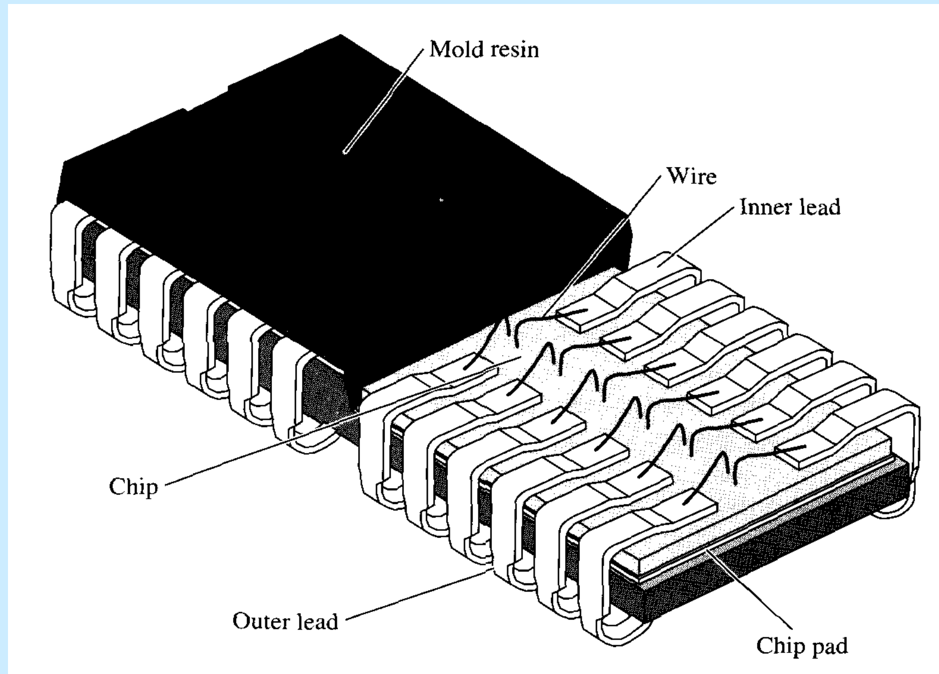


Pin grid array (**PGA**) multilayer ceramic package containing 10 ceramic layers and 132 pins

Through – Hole Package

- Available in hermetic–ceramic and plastic types
- Easier placement for soldering and stronger solder joints at the printed circuit board (PWB) level
- Sacrificing PWB design flexibility, restricting mounting density because of the fine–pitch drilling process, and adding drilling cost

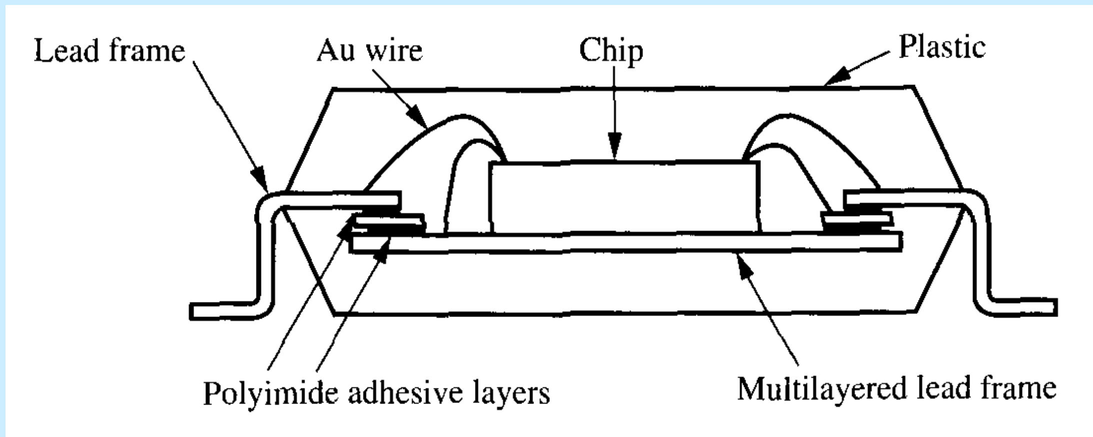
Surface – Mount Package



Surface–mount lead–on–chip package structure: Tips of the lead frame extend above the chip center where the bonds are made

In memory devices where comparatively smaller pin counts are required, the J-lead package is a frequent choice. The soldering portions of J-leads are located beneath the plastic body, and so they do not need extra space for soldering as gull-wing leads do, thus decreasing the overall area the package occupies.

Surface – Mount Package



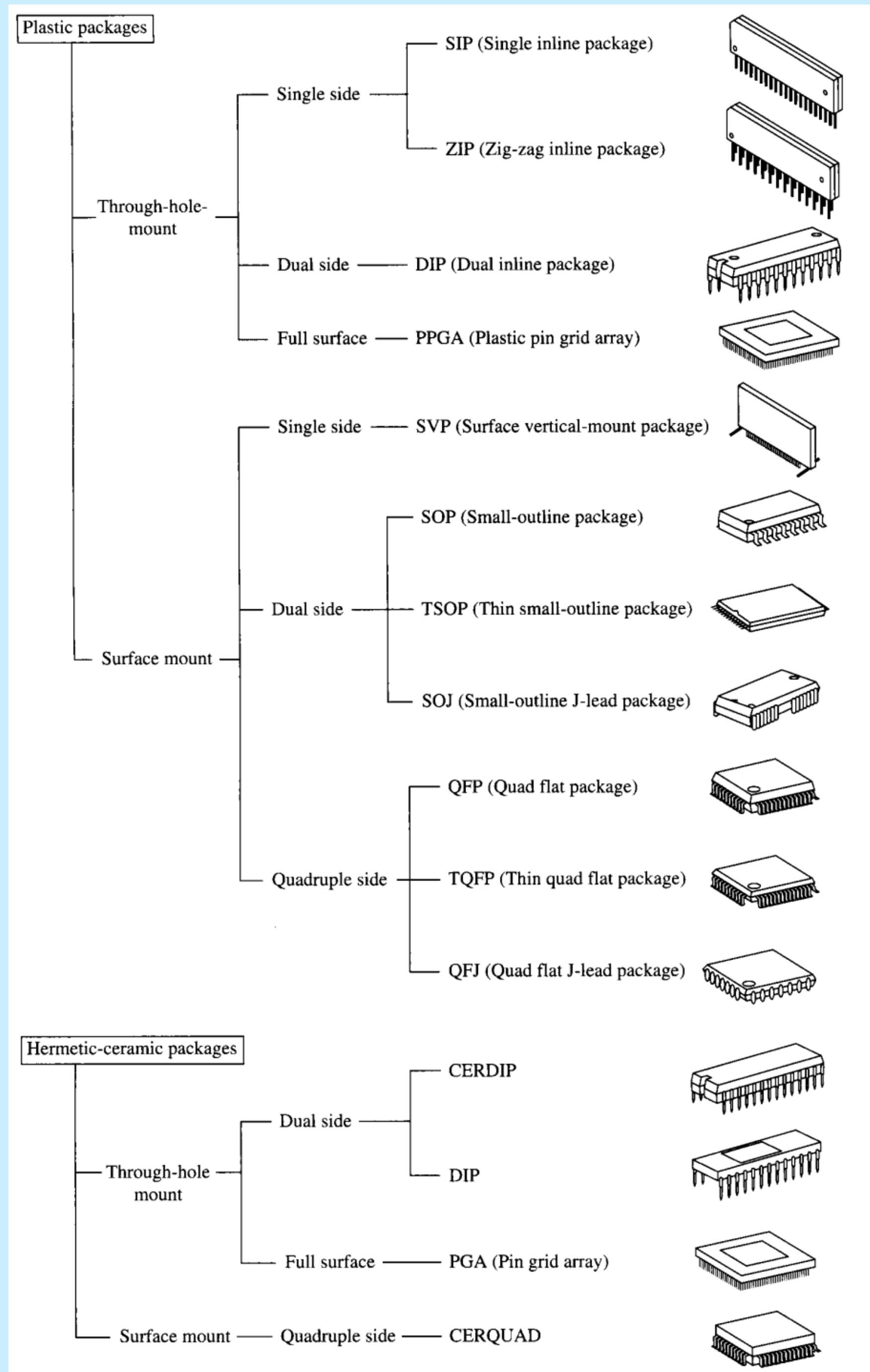
Multilayer lead frame package: The ground plane that also serves as the chip support paddle and the power plane are attached to the lead frame with electrically insulating adhesives

Gull-wing leads are easier to form than J-leads, and the better geometry integrity of the leads is particularly suitable for higher pin count and finer pitch areas.

Surface – Mount Package

- Over 50% of packages used today are of the surface–mount (SM) type
- Although SM packages include hermetic–ceramic and plastic types, the cheaper plastic package is preferred because the package cost increases with the pin counts
- SM packages enhance PWB design flexibility because through–holes are unnecessary, allowing finer pitch soldering than TH packages as the pitch is determined by the PWB (Cu foil) etching process in lieu of the drilling requirements
- Generally, SM packages provide better area efficiency

Common IC Packages



Tape Carrier Package (TCP) – Tape Automated Bonding (TAB)

Type	Structure
One-layer	Metal foil, Bump, Chip
Two-layer	Metal foil, Bump, Chip, Film
Three-layer	Metal foil, Bump, Chip, Film, Adhesive
Bumped tape	Metal foil, Al pad, Chip, Bump, Film, Adhesive

- The one-layer tape carrier is a thin Cu foil, and even though it is cost effective, it is not preferred nowadays
- A two-layer tape has a 25 µm Cu layer on a polyimide base tape typically 75 µm thick
- A three-layer tape is similar to the two-layer structure but has an additional adhesive layer between the Cu and the base plastic layer

Tape automated bonding is performed by:

- Bonding to the bumps on the chip using one to three layer tapes
- Bonding to Al pads on the chip using a bumped tape
- Former method is more popular in the IC industry