

CHAPTER 11: Testing, Assembly, and Packaging

The previous chapters focus on the fabrication of devices in silicon or the front-end technology. Hundreds of chips can be built on a single wafer, and even though the processing steps are complex and expensive, the use of batch technology enables mass production and makes the ultimate cost of each chip fairly low. In this chapter, we will concentrate on some of the back-end technologies, namely testing, assembly, and packaging. Comparing to the dramatic front-end processes, the processes of attaching leads and packaging the devices could seem rather mundane. However, such an impression would be far from accurate since the techniques discussed in this chapter are crucial to the overall fabrication process. In fact, the handling and packaging of individual circuits can be the most critical steps of all from the viewpoints of cost and reliability. The individual IC chip must be connected properly to outside leads and packaged in a way convenient for use in a larger circuit or system. Since the devices are handled individually once they are separated from the wafer (*Figure 11.1*), bonding and packaging are expensive processes.

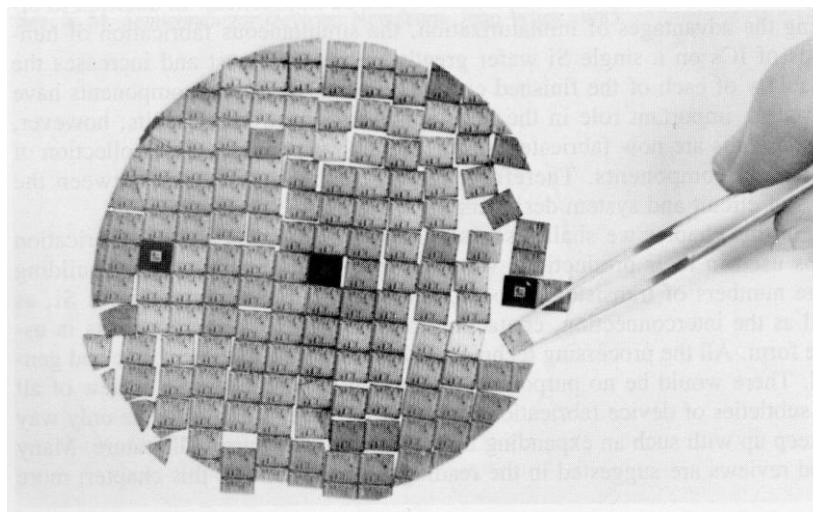


Figure 11.1: A wafer of integrated circuits after scribing and breaking into individual chips.

11.1 Testing

After the wafer has been processed and the final metallization pattern defined, it is placed in a holder under a microscope and is aligned for testing by a multiple-point probe (*Figure 11.2*). The probe contacts the various pads on an individual circuit and a series of tests are made of the electrical properties of the device. The various tests are conducted automatically in a very short time ranging from a few milliseconds for a simple circuit to 30 seconds or more for a complex chip. The test results are fed into a computer, and a decision is made regarding the acceptability of the circuit. If the chip is defective or the circuit falls below specifications, the computer instructs the test probe to mark the circuit with a dot of ink. The probe automatically steps the prescribed distance to the next chip on the wafer and repeats the process. After all of the circuits have been tested and substandard ones marked, the wafer is removed from the testing machine, scribed between the circuits, and broken apart (see *Figure 11.1*). In the testing process, information from tests on each circuit can be printed out to facilitate analysis of the rejected ones or to evaluate the fabrication process for possible modification.

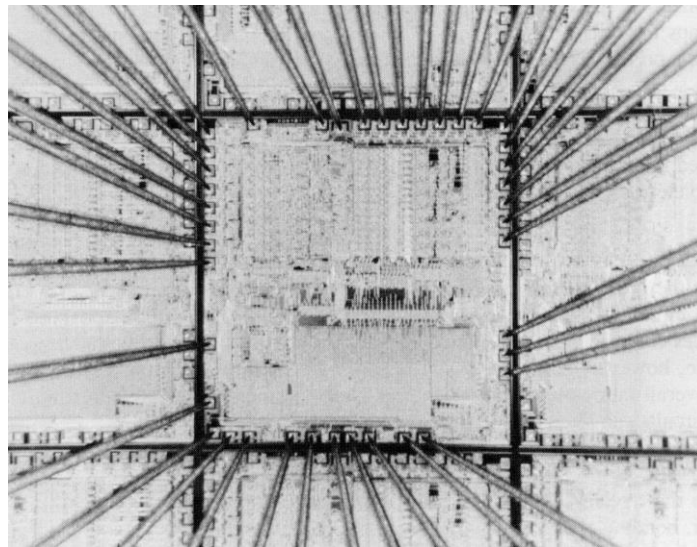


Figure 11.2: An integrated circuit under test by a multiple-point probe. In this example, 40 test probes touch the contact pads of this chip about 0.5 cm on a side. The probes are rigidly fixed in position, so that the wafer can be stepped to the next circuit with little realignment.

11.2 Wafer Preparation

Wafer preparation starts with the back-grinding process at the end of the wafer fabrication process. For example, 150 mm diameter wafers are thinned from 650 μm to approximately 400 μm thick. Wafers are then mounted to an adhesive tape and a dicing saw with a diamond blade separates wafers into individual chips (see [Figure 11.1](#)). Wafer dicing machines are completely automatic and contain features such as alignment systems, integrated cleaning stations, drying ovens, and quality monitoring tools. The separated chips, still mounted in the tape – frame fixtures, are subsequently sorted by recognizing the bad chip marks or by reading the positional mapping data from the wafer testing equipment.

11.3 Die Bonding and Wire Bonding

Before the chip is wire bonded, it is first mounted solidly on a metal lead frame (*Figure 11.3*) or on a metallized region of an insulating substrate. In this process, a thin layer of Au (perhaps combined with Ge or other elements to improve the metallurgical contact) is placed between the bottom of the chip and the substrate. Heat and a slight scrubbing motion are applied to form an alloyed bond holding the chip firmly to the substrate. This process is called die bonding. Once the chip is mounted, interconnecting wires are attached from the various contact pads on the IC to the posts on the lead frame (*Figure 11.4*), a process termed wire bonding.

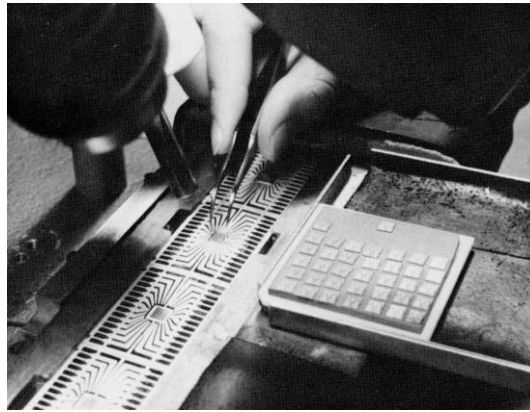


Figure 11.3: Mounting of chips in metal lead frames, in preparation for die bonding and contacting steps. The process is usually automated.

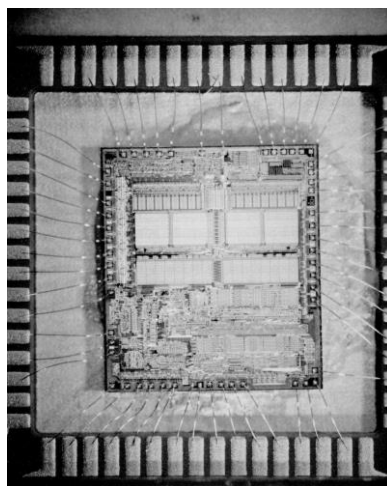


Figure 11.4: Attachment of leads from the Al pads on the periphery of the chip to posts on the package.

In Au wire bonding, a spool of fine Au wire 20 to 50 μm in diameter is mounted in a lead bonder apparatus, and the wire is fed through a glass or tungsten carbide capillary (*Figure 11.5a*). A hydrogen gas flame jet is swept past the wire to form a ball on the end. In thermocompression bonding, the chip (or in some cases the capillary) is heated to about 360°C , and the capillary is brought down over the contact pad. When pressure is exerted by the capillary on the ball, a bond is formed between the Au ball and the Al pad (*Figure 11.5b*). Then, the capillary is raised and moved to a post on the lead frame. The capillary is brought down again, and the combination of force and temperature bonds the wire to the post. After raising the capillary again, the hydrogen flame is swept past, forming a new ball (*Figure 11.5c*), and the process is automatically repeated for other pads on the chip.

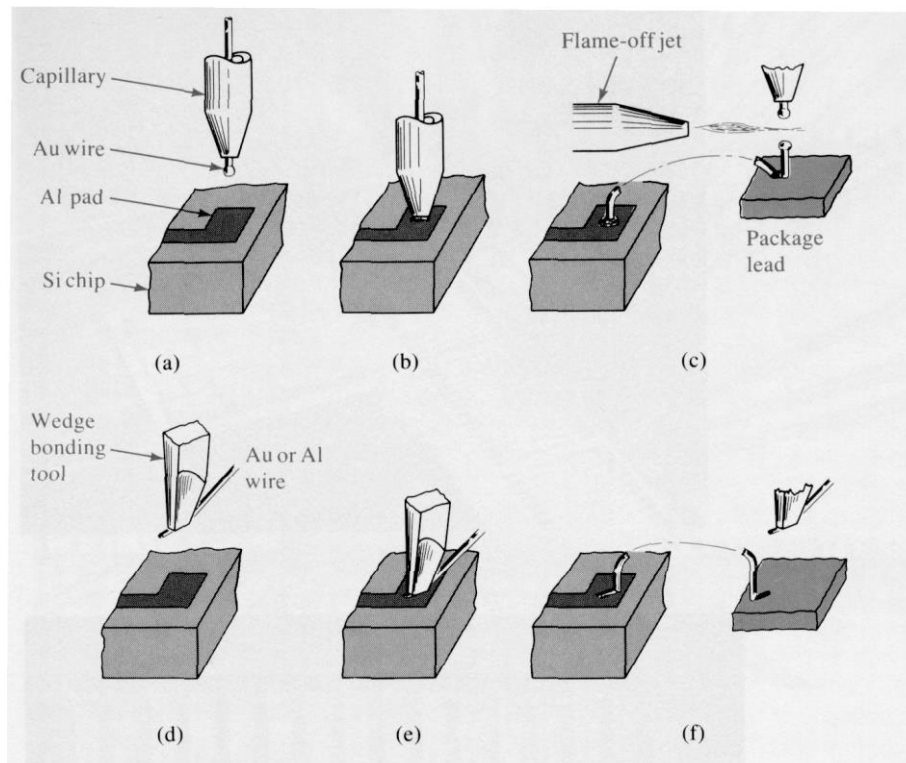


Figure 11.5: Wire bonding techniques: (a) Capillary positioned over one of the contact pads for a ball (nail-head) bond. (b) Pressure exerted to bond the wire to the pad. (c) Post bond and flame-off. (d) Wedge bonding tool. (e) Pressure and ultrasonic energy applied. (f) Post bond completed and wire broken or cut from next bond.

There are many variations in this basic method. For example, substrate heating can be substituted by ultrasonic bonding. In this method, a tungsten carbide capillary is held by a tool connected to an ultrasonic transducer. When it is in contact with a pad or a post, the wire is vibrated under pressure to form a bond. Other options include techniques for automatically removing the tail left on the post as shown in [Figure 11.5c](#). Aluminum wires can be used in ultrasonic bonding. Al has several advantages over Au, including the absence of possible metallurgical problems in bonds between Au and Al pads. When an Al wire is used, the flame-off step is replaced by cutting or breaking the wire at the appropriate points. In forming a bond, the wire is bent under the edge of a wedge-shaped bonding tool ([Figure 11.5d](#)). The tool then applies pressure and ultrasonic vibration to form the bond ([Figures 11.5e](#) and [11.5f](#)). The resulting flat bond is called a wedge bond ([Figure 11.6](#)).

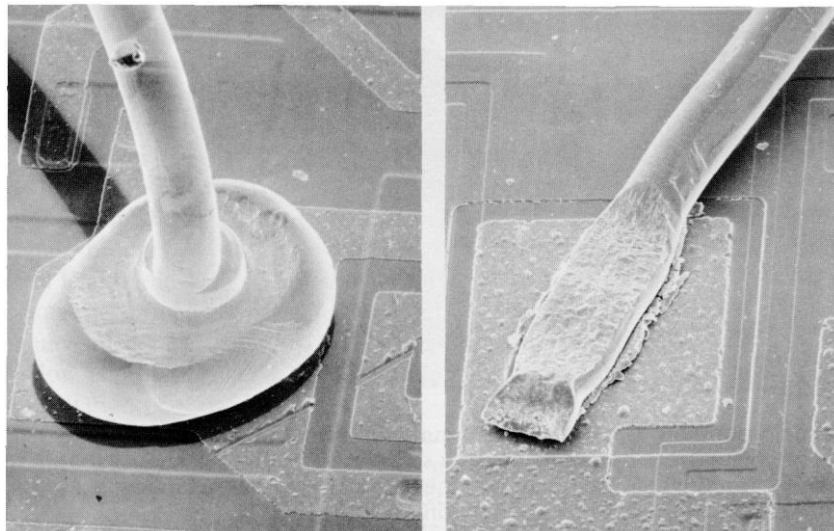


Figure 11.6: Scanning electron micrographs of a ball bond (left) and wedge bond (right).

11.4 Flip-Chip Technique

The time consumed in bonding wires individually to each pad on the chip can be overcome by several methods utilizing simultaneous bonding, such as the flip-chip approach. In this case, relatively thick metal is deposited on the contact pads before the devices are separated from the wafer. After separation, the deposited metal is used to contact a matching metallized pattern on the package substrate.

In the flip-chip method, bumps of solder or special metal alloys are deposited on each contact pad. These metal bumps rise about 50 μm above the surface of the chip. After separation from wafer, each chip is turned upside down, and the bumps are properly aligned with the metallization pattern on the substrate. At this point, ultrasonic bonding or solder alloying attaches each bump to its corresponding connector on the substrate (*Figure 11.7*). An obvious advantage of this method is that all connections are made simultaneously. Disadvantages include the fact that the bonds are made under the chip and therefore cannot be inspected visually. Furthermore, it is necessary to heat and / or exert pressure on the chip.

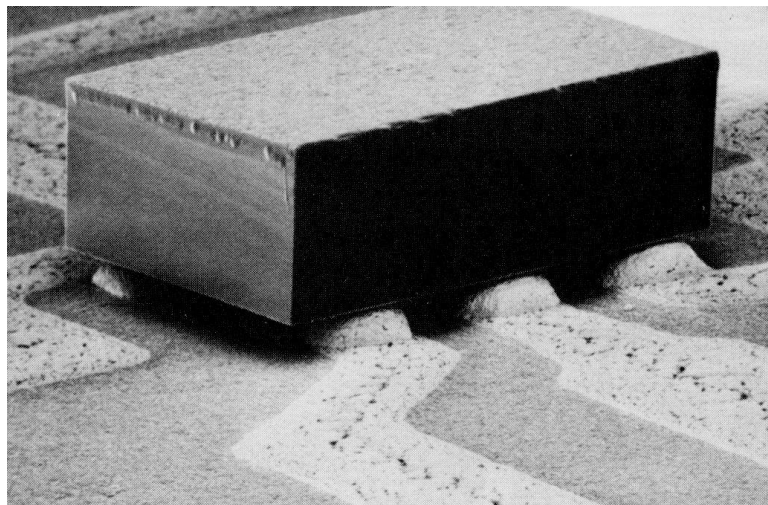


Figure 11.7: Flip-chip bonding. The integrated circuit chip is mounted directly on the thick-film substrate by simultaneously soldering a number of metallized bumps on the chip to the interconnection patterns on the substrate.

11.5 Hermetic and Plastic Packages

The final step in IC fabrication is packaging the device in a suitable medium that can protect it from the environment of its intended application. In most cases, this means the surface of the device must be isolated from moisture and contaminants and the bonds and other elements must be protected from corrosion and mechanical shock.

Package types are divided into two categories: hermetic–ceramic and plastic. In a hermetic package, the chip resides in an environment decoupled from the external environment by a vacuum tight enclosure. The package is usually ceramic based and designed for high performance applications that allow some cost penalties. In a plastic package, on the other hand, the chip is not perfectly isolated from the external environment because it is encapsulated with resin materials, typically epoxy based resin. The outside ambient affects the chip over time and gradually penetrates the plastic. Plastic packages have become more popular as their applications expand and the technology improves.

Figure 11.8 illustrates a typical hermetic package. The chip resides in a cavity of the package. The package material is a formed ceramic on which metal wirings and external leads are placed. The chip and package are interconnected by fine Al wires. Hermetic sealing is complete with the cap, usually ceramic or metal, lidded to the package. The package excludes environmental contaminants and has little mechanical or chemical effect on the chip, since the package components do not touch the chip surface. Al_2O_3 is the usual ceramic material, and AlN is used when higher power dissipation is required.

Figure 11.9 depicts a typical plastic package. The chip is attached to the paddle of the lead frame. The frame, made of etched or stamped thin metal (usually Fe-Ni or Cu alloys), serves as a skeleton around which the package is assembled, and it provides external leads in the completed package. Interconnections are fine gold wires. Encapsulation is accomplished by molding using epoxy resin that covers the chip and forms the outer shape of the package at the same time. External leads are formed into the final shape after molding. The package cannot thoroughly decouple the chip from the environment, and so the mechanical and chemical effects from the plastic touching the chip require attention.

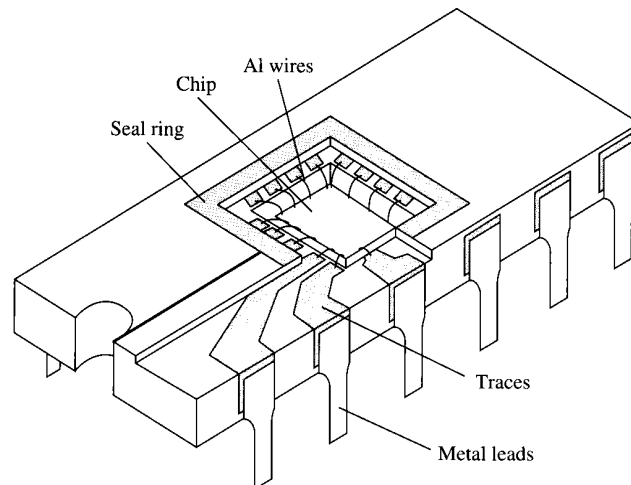


Figure 11.8: Schematic of a typical hermetic package. A silicon chip is placed in the cavity of a ceramic package and wedge bonded to make electrical connections to the terminals on the package. Metallized traces, usually of W, form electrical paths on the package. Lid sealing makes the cavity hermetic.

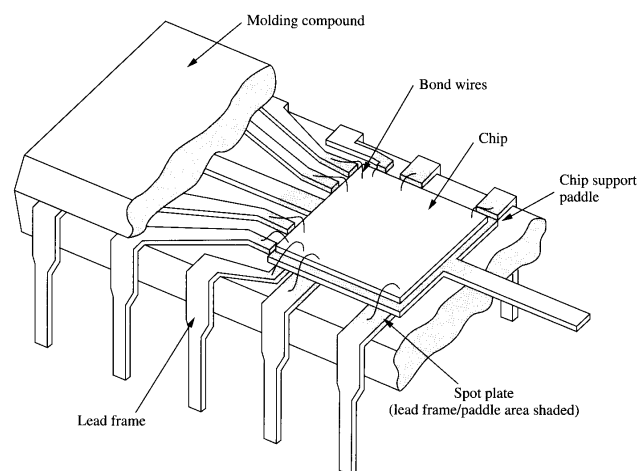


Figure 11.9: Schematic of a typical plastic package. The package is a composite structure consisting of a silicon chip, a metal lead frame, and a plastic molding compound. The chip support paddle and inner tips of the lead frame are Ag plated. External leads are solder plated after molding.

11.6 Through-Hole and Surface-Mount Packages

Next-level packaging, particularly at the printed wiring board (PWB) level, classifies single chip packages into through-hole (TH) and surface-mount (SM) types. The TH types include the dual-in-line package (DIP) shown in [Figure 11.10](#) and the pin-grid-array (PGA) package displayed in [Figure 11.11](#). Both are available in hermetic-ceramic and plastic types. TH packages provide easier placement for soldering and stronger solder joints at the PWB level. However, they sacrifice PWB design flexibility, restrict mounting density because of the fine-pitch drilling process, and add drilling cost.

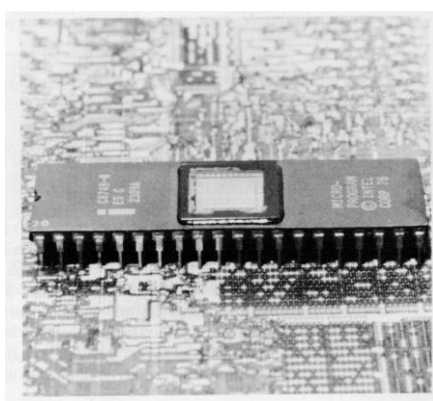


Figure 11.10: Packaging of a microcomputer chip in a DIP. A transparent lid is included over the chip for erasure of the EPROM (electrically programmable read only memory) by ultraviolet light.

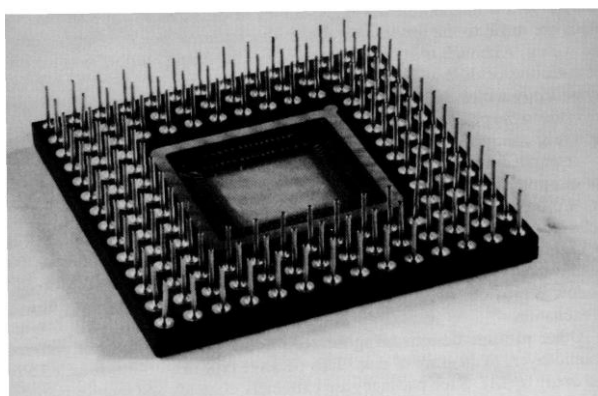


Figure 11.11: A pin grid array (PGA) multilayer ceramic package containing 10 ceramic layers and 132 pins.

Over 50% of packages used today are of the surface-mount (SM) type. Although SM packages include hermetic-ceramic and plastic types, the cheaper plastic package is preferred because the package cost increases with the pin counts. SM packages enhance PWB design flexibility because through-holes are unnecessary. They allow finer pitch soldering than TH packages do, as the pitch is determined by the PWB (Cu foil) etching process in lieu of the drilling requirements. Generally, SM packages provide better area efficiency. SM packages come in two different geometric forms: J-leads shown in [Figure 11.12](#) and gull-wing leads exhibited in [Figure 11.13](#). In memory devices where comparatively smaller pin counts are required, the J-lead package is a frequent choice. The soldering portions of J-leads are located beneath the plastic body, and so they do not need extra space for soldering as gull-wing leads do, thus decreasing the overall area the package occupies. However, for logic and microprocessor chips, high pin counts are required and gull-wing leads predominate. Gull-wing leads are easier to form than J-leads, and the better geometry integrity of the leads is particularly suitable for higher pin count and finer pitch areas.

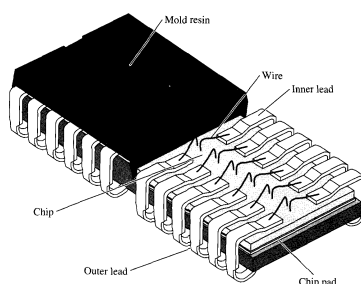


Figure 11.12: Schematic of a surface-mount lead-on-chip package structure. Tips of the lead frame extend above the chip center where the bonds are made.

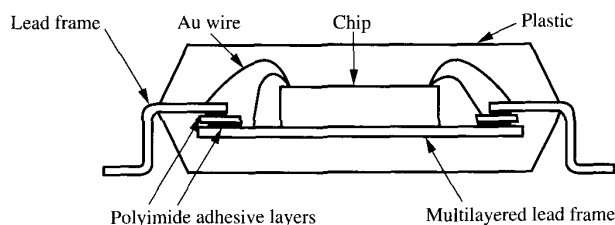


Figure 11.13: Multilayer lead frame package that provides large area power and ground planes. The ground plane, which also serves as the chip support paddle, and the power plane are attached to the lead frame with electrically insulating adhesives. Many bonds are made from pads on the chip to these planes.

Many package variations exist in the industry. *Figure 11.14* displays some of the common IC packages.

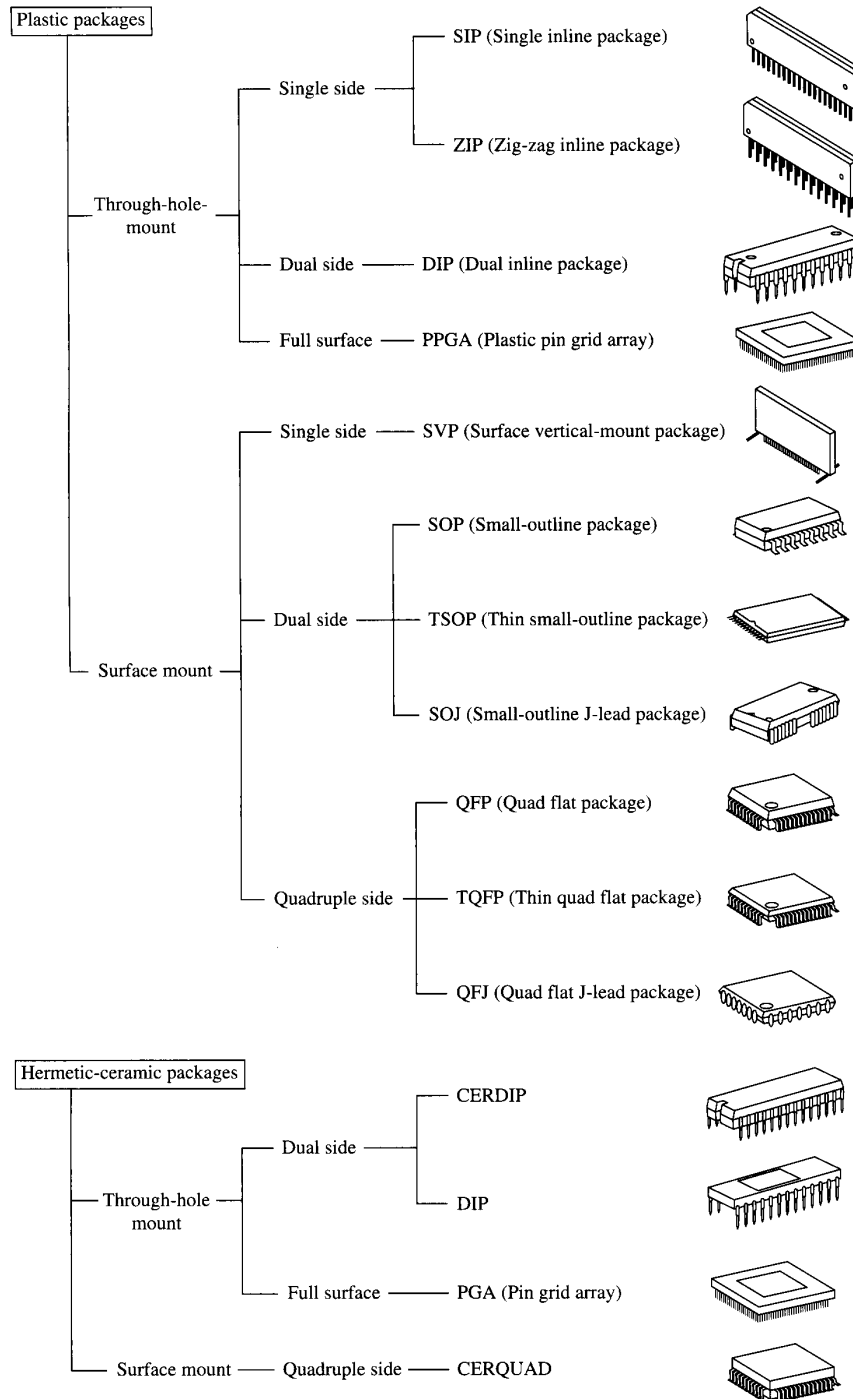


Figure 11.14: Common IC packages.

11.7 Tape Carrier Packages

Tape carrier package (TCP) is a generic term for packages in which a tape automated bonding (TAB) technique is used for the pads-on-chip interconnects. *Figure 11.15* depicts typical tape carriers used in TCP fabrication. The one-layer tape carrier is a thin Cu foil, and even though it is cost effective, it is not preferred nowadays. A two-layer tape has a 25 μm Cu layer on a polyimide base tape typically 75 μm thick. A three-layer tape is similar to the two-layer structure but has an additional adhesive layer between the Cu and the base plastic layer. Tape automated bonding is performed by: (i) bonding to the bumps on the chip using one to three layer tapes, or (ii) bonding to Al pads on the chip using a bumped tape. The former method is more popular in the IC industry.

Type	Structure
One-layer	<p>Metal foil</p> <p>Bump</p> <p>Chip</p>
Two-layer	<p>Metal foil</p> <p>Film</p> <p>Bump</p> <p>Chip</p>
Three-layer	<p>Metal foil</p> <p>Film</p> <p>Adhesive</p> <p>Bump</p> <p>Chip</p>
Bumped tape	<p>Metal foil</p> <p>Film</p> <p>Adhesive</p> <p>Bump</p> <p>Al pad</p> <p>Chip</p>

Figure 11.15: Cross section of typical tape carriers used in TCP fabrication.