Chapter 10

Metallization

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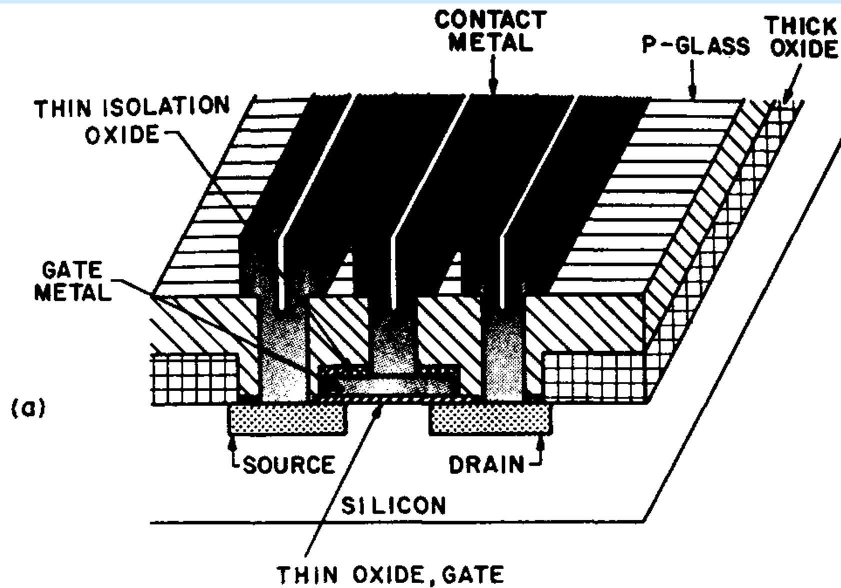
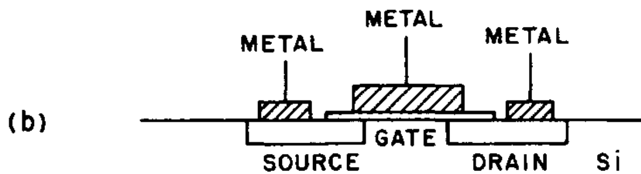
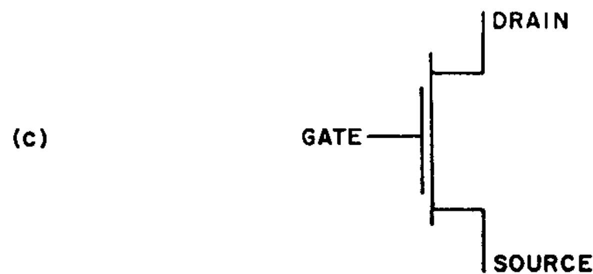






Polysilicon and silicide are frequently used in gates and interconnects in MOS devices

Aluminum and copper are the metals of choice as contact and second-level interconnection to the outside

Desired properties of the metallization for integrated circuits

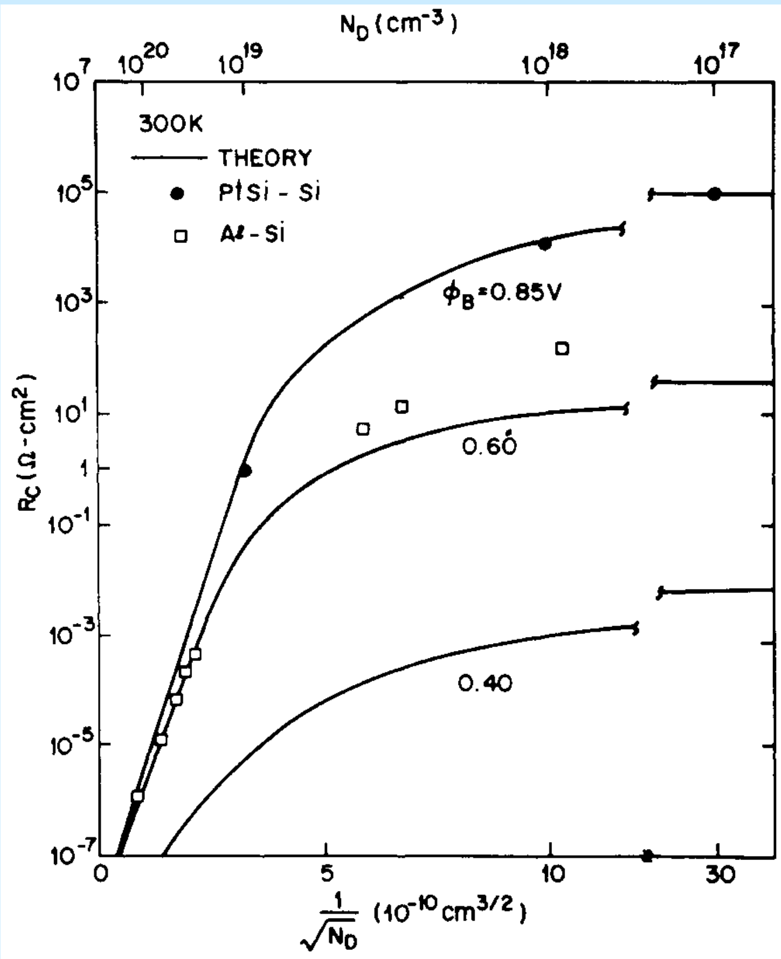
- Low resistivity
- Easy to form
- Easy to etch for pattern generation
- Stable in oxidizing ambient and oxidizable
- Mechanical stability, good adherence, and low stress
- Surface smoothness
- Good device characteristics and lifetimes

Desired properties of the metallization for integrated circuits

- Stability throughout processing, including high temperature sintering, dry or wet oxidation, gettering, phosphorus glass (or any other materials) passivation, and metallization
- No reaction with final metals
- Not contaminating devices, wafers, or apparatus
- For window contacts - low contact resistance, minimal junction penetration, and low electromigration

- The circuit speed is dictated by the resistance and capacitance of the interconnection runners
- Metallization dictates the flat-band voltage V_{FB}:

  $V_{FB} = \Phi_m - \Phi_s = \Phi_{ms}$, where Φ_m is the work function of the gate metallization and Φ_s is the work function of the semiconductor
- V_{FB} contributes to the threshold voltage V_T which designates the voltage required at the gate metal to achieve conduction between the source and drain regions



- A good ohmic contact is electrically and mechanically stable
- The contact resistance R_C should be negligible
- R_C is related to the Schottky barrier height of the metal Φ_B and the dopant density N
- The Schottky barrier between the metal and semiconductor stems from the requirement that the Fermi levels in the two materials must align at the interface

R_C diminishes with increasing dopant concentration and decreasing barrier height

Possible metallization choices

Application	Choices
Gates and interconnection and contacts	Polysilicon, silicides, nitrides, copper, refractory metals, aluminum, and combinations of two or more of above
Diffusion barrier	Ti, TiN, Ta, TaN, Ti-W alloy, silicides
Top level	Aluminum, copper
Selectively formed metallization on silicon only	Some silicides, tungsten, aluminum, copper

Aluminum Metallization

- Aluminum on silicon or silicide can lead to deleterious metallurgical interaction
- Annealing of aluminum on silicon at 450°C causes dissolution of silicon into the metal and leads to pit formation
- If this penetration is deep, contact and junction failure can result
- A useful solution is to dope the Al with approximately 1 wt. % Si thereby reducing diffusion of silicon from the underlying substrate

- The problem is not totally circumvented if the contact is fabricated on n-type silicon, because the excess amount of silicon present in aluminum can, upon cooling, precipitate in the contact, leading to nonohmic contact to n-type silicon because the crystallized silicon precipitates contain aluminum which is a p-type dopant
- A diffusion barrier such as titanium nitride is applied between the aluminum metallization and the silicon substrate
- Generally, a thickness on the order of 50 to 100 nm is sufficient

Electromigration

- Electromigration, which causes considerable material transport in metals, occurs because of enhanced and directional mobility of atoms under the influence of an electric field
- Electromigration in aluminum is known to result in voids which are manifested by discontinuities in the metallization runners and pileups that can short-circuit adjacent conductors
- The electromigration resistance can be increased by alloying with copper (~ 0.5%)

Physical Vapor Deposition

- The common forms of physical vapor deposition (PVD) are evaporation, e-beam evaporation, plasma spray deposition, and sputtering
- Evaporation and e-beam evaporation used to be the workhorses in the IC industry but sputtering is now the dominant PVD technique in the industry

Advantages of Sputtering

- High deposition rate afforded by modern cathode and target design
- Capability to deposit and maintain complex alloy compositions
- Ability to deposit high-temperature and refractory metals
- Capability to maintain well-controlled, uniform deposition on large (200 mm and larger) wafers
- Ability, in multi-chamber systems, to clean the contact before depositing metal

Mechanism of Sputtering

- Sputtering is usually carried out in an argon plasma and by biasing the target (source of metal) negatively, argon ions are attracted to the target
- The momentum of the Ar ions is transferred to the target resulting in the ejection of one or more atoms from the surface of the target
- The sputtered atoms, mostly neutral, fly into the plasma and land on the wafer

- Like evaporation, sputter deposition occurs essentially along a line-of-sight path with a cosine distribution
- Poor step coverage can result if the surface topography of the wafer is abrupt
- The uniformity of the deposited film can be improved by raising the substrate temperature (enhancing surface migration), using a larger target, or inserting a collimator between the sputtering cathode and wafer

Reactive Ion Sputtering

- Reactive sputtering of titanium nitride is conducted by introducing nitrogen into the Ar plasma in the sputtering chamber

- The plasma provides enough energy to dissociate the nitrogen molecules into atomic nitrogen, which subsequently reacts with Ti to form titanium nitride

Chemical Vapor Deposition

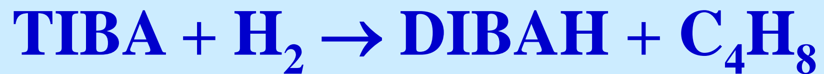
- Excellent step coverage
- Large throughput
- Low-temperature processing
- A number of metals and metal compounds, such as Al, Cu, WSi_2, TiN, and W, can be deposited by chemical reaction or thermal decomposition of precursors
- Usually the wafer needs to be heated to 100°C to 800°C to provide the initial thermal energy to overcome the reaction barrier

Plasma CVD

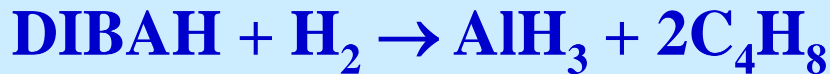
- The advantage is that the energy required to overcome the initial reaction barrier can be supplied by the plasma, and the deposition temperature can be decreased.
- This reduction is especially important for metal or metal compounds used for vias and multilevel interconnects since their tolerance for high temperature is limited

CVD Aluminum

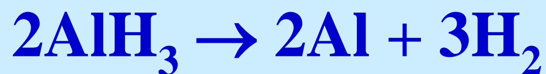
Al can be deposited using CVD precursors such as tri-isobutyl-Al, $(C_4H_9)_3Al$, or TIBA:



$$\text{TIBA} + H_2 \rightarrow \text{DIBAH} + C_4H_8$$



$$\text{DIBAH} + H_2 \rightarrow AlH_3 + 2C_4H_8$$



$$2AlH_3 \rightarrow 2Al + 3H_2$$

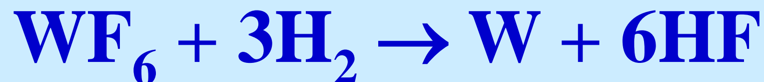
DIBAH stands for di-isobutyl Al hydride or $(C_4H_9)_2AlH$

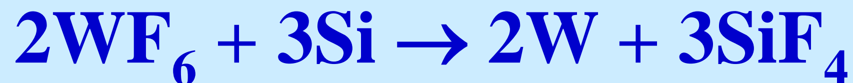
The first reaction occurs at 40°C to 50°C before the gas reaches the wafer and the second one occurs on the wafer heated to 150°C to 300°C. In practice, DIBAH is the chemical precursor decomposing on the wafer surface, but the direct use of DIBAH is impractical due to its low vapor pressure and deposition rate

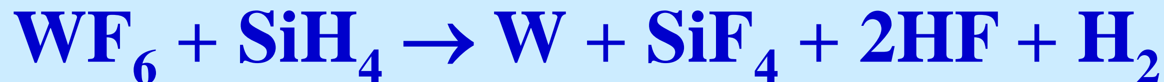
- A problem with CVD Al is that there is no Cu in the materials to boost the electromigration resistance
- A simple solution is to deposit ~50% of the total thickness of Al by CVD and the rest by sputtering of Al-Cu alloy. Subsequent heating to 250°C to 400°C allows the Cu in the alloy to redistribute to the entire Al wiring
- Alternatively, CVD Al can be deposited with simultaneous Cu doping using dimethyl aluminum hydride (DMAH) and cyclopentadienyl copper triethylphosphine (CpCuTEP)

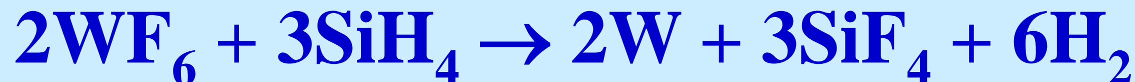
CVD Tungsten

CVD W is used both as a contact plug and first-level metal. The basic chemistry of CVD W is:





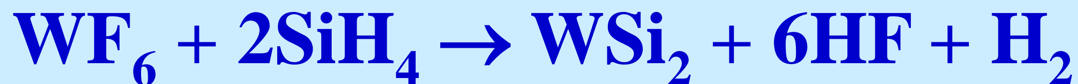




- During CVD W deposition, the wafer is held on a heated chuck between 400°C and 500°C and opposite to an orifice where the WF_6, H_2, or SiH_4 gases are injected
- SiH_4 is first introduced without WF_6 to initiate the deposition of a very thin layer (a few nanometers) of amorphous Si as a prenucleation layer, followed by a [SiH_4 + WF_6] silane reduction nucleation process and a high-rate [H_2 + WF_6] hydrogen reduction deposition
- At the nucleation stage, less than 100 nm of W is deposited and the bulk of the W deposition is by hydrogen reduction

CVD Tungsten Silicide

WSi_2 is used widely on top of gate polysilicon to form a low-resistance polycide gate. CVD WSi_2 is readily deposited using the silane reduction of WF_6 at 300°C to 400°C:



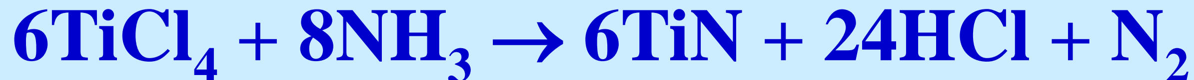
$$WF_6 + 2SiH_4 \rightarrow WSi_2 + 6HF + H_2$$

In a CVD reactor, the flow rates of WF_6 and SiH_4 control the outcome of the reaction. A higher SiH_4 to WF_6 ratio results in WSi_2 deposition. In practice, a ratio greater than 10 is used to ensure the deposition of WSi_x ($x = 2.2$ to 2.6).

WSi_2 can also be deposited by dichlorosilane (SiH_2Cl_2 or DCS) reduction at 500°C to 600°C:

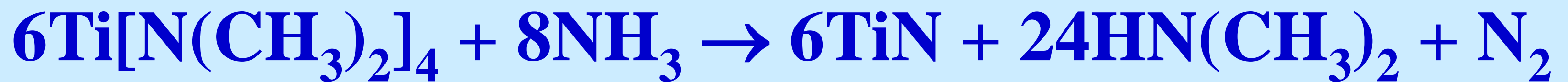
CVD Titanium Nitride

TiN is widely used as a barrier metal layer for CVD W deposition. CVD TiN can provide better coverage than PVD methods and is more economical than collimated sputtering. CVD TiN can be deposited using $TiCl_4$ and NH_3, H_2 / N_2, or NH_3 / H_2:



- The deposition temperature is 400°C to 700°C for NH_3 reduction and less than 700°C for the N_2 / H_2 reaction
- Generally, the higher the deposition temperature, the better the TiN film and less Cl incorporated into the TiN
- Even the best TiN produced by this process contains about 0.5% Cl
- The lower temperature processes result in even higher Cl (~ 5%) causing concerns about the corrosion reliability of the Al wiring

TiN can be deposited using metal-organic precursors that are usually in the form of a Ti-alkylamine complex. One example is the use of tetrakis-(dimethylamido)-Ti [also written as TDMAT or $Ti(NMe_2)_4$] and NH_3:



$$6Ti[N(CH_3)_2]_4 + 8NH_3 \rightarrow 6TiN + 24HN(CH_3)_2 + N_2$$

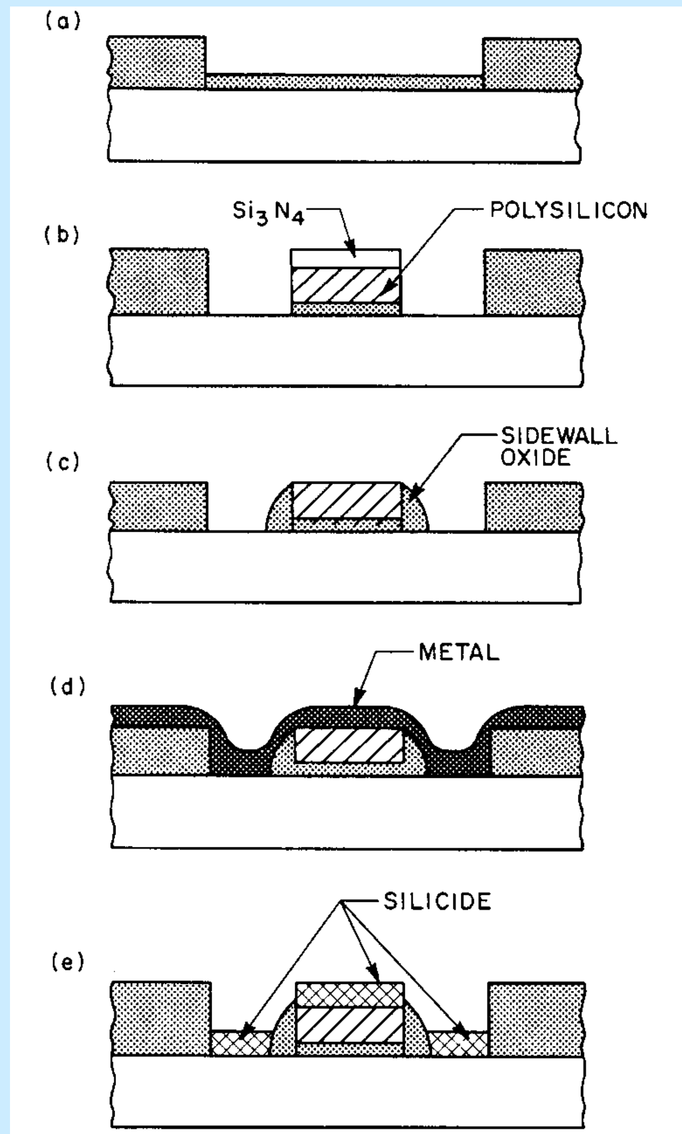
TiN deposition by metal-organic precursors can be done at low temperature ($\leq$ 450°C) and imposes no danger of Cl incorporation. However, C and O inclusion can give rise to high resistivity.

CVD Copper

- Because of its low resistivity and good electromigration resistance, Cu metallization is more desirable than Al in some applications
- There are two types of metal-organic precursors for Cu: the divalent Cu^{II} in the form of $Cu^{II}(\beta\text{-diketonate})_2$ and the monovalent Cu^{I} in the form of $Cu^{I}(\beta\text{-diketonate})L$ where L is a neutral ligand weakly bonded to Cu
- The most commonly used Cu^{II} precusor is bis-hexafluoroacetyl-acetonate-Cu^{II} or $Cu(hfac)_2$
- High deposition rates and good quality films are achieved by hydrogen reduction

- Copper lacks a dense oxide and is thus vulnerable to corrosion
- Like Au, Cu can diffuse through SiO_2 and cause deep impurity levels in Si, reducing bipolar gain and causing junction leakage
- Cu has no volatile compounds at room temperature and thus cannot be etched by the RIE process at moderate temperature ($\leq 200^{o}C$)
- The use of Cu as interconnects depends on issues well beyond the deposition techniques
- To prevent corrosion and Cu diffusion into Si, a cladding layer such as TiN or Ta is needed

Self-Aligned Silicide (SALICIDE)

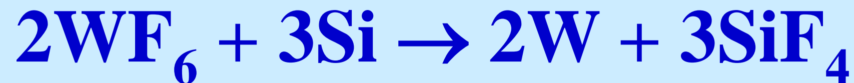


CVD Metal Plug

- One of the difficult problems in metallization is to ensure enough metal continuity at contact windows and vias
- The step coverage of sputtered Al degrades rapidly with increasing contact window aspect ratio, and at small design rules, the step coverage at contacts and vias drops below 20%
- Various forms of metal plugs have been developed

Selective CVD Tungsten Plug

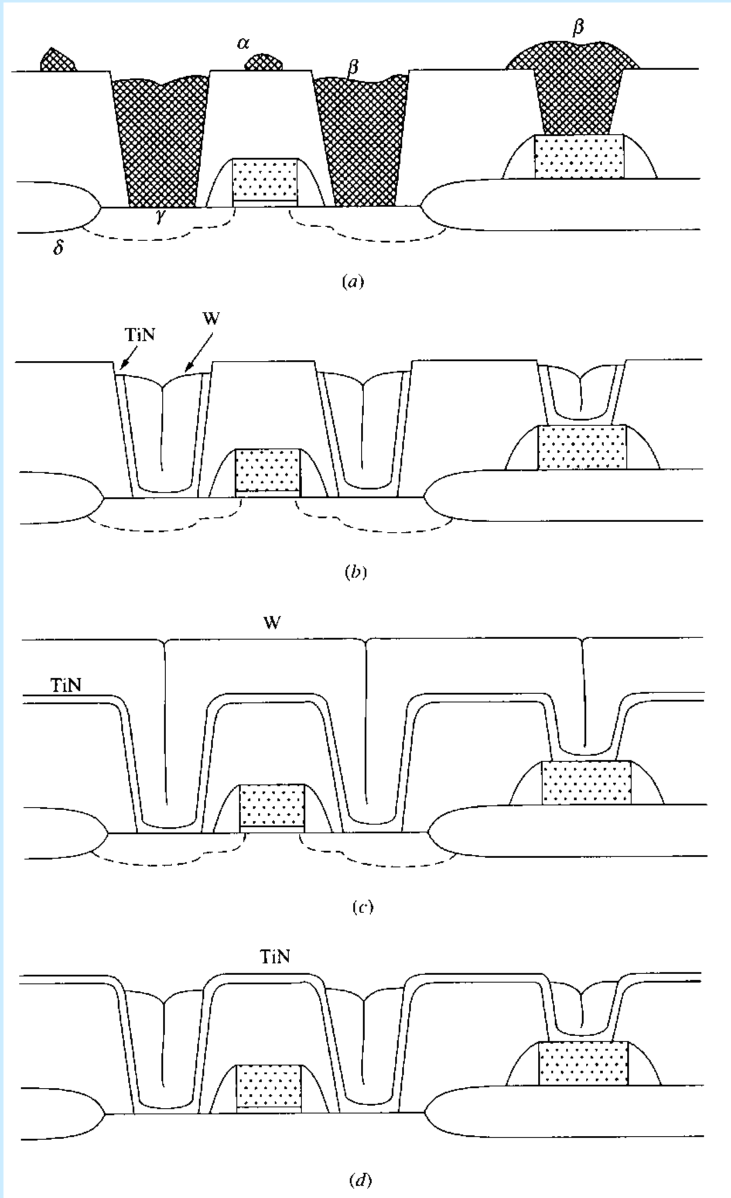
The selective CVD W plug process starts on a Si contact from a Si reduction process:



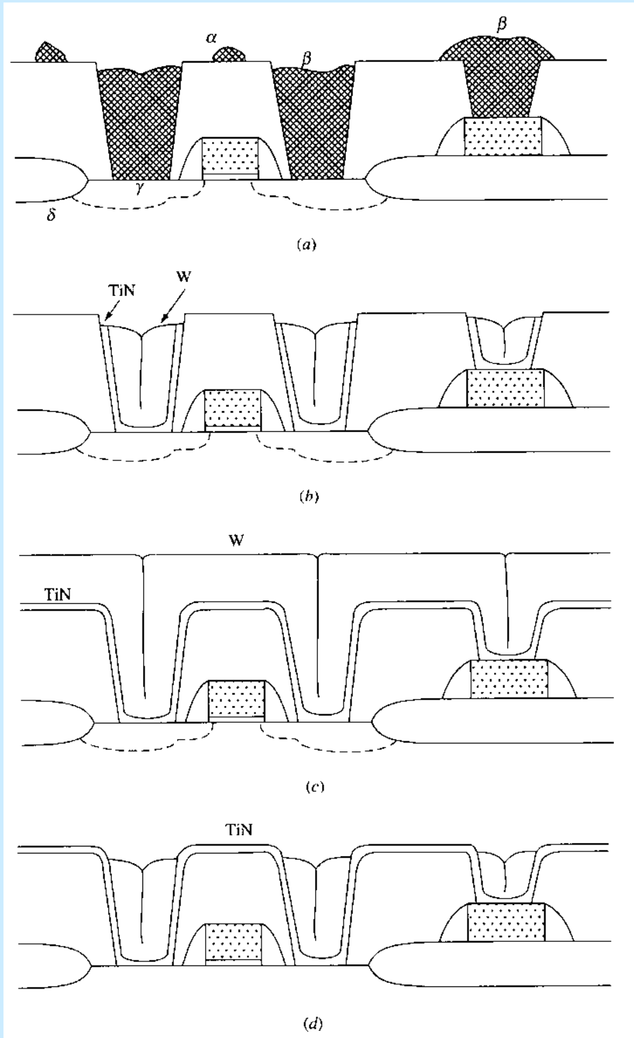
$$2WF_6 + 3Si \rightarrow 2W + 3SiF_4$$

This process provides a nucleation layer of W grown on Si but not on SiO_2. The real W plug is grown by the following hydrogen reduction process that deposits W rapidly on the nucleation layer:

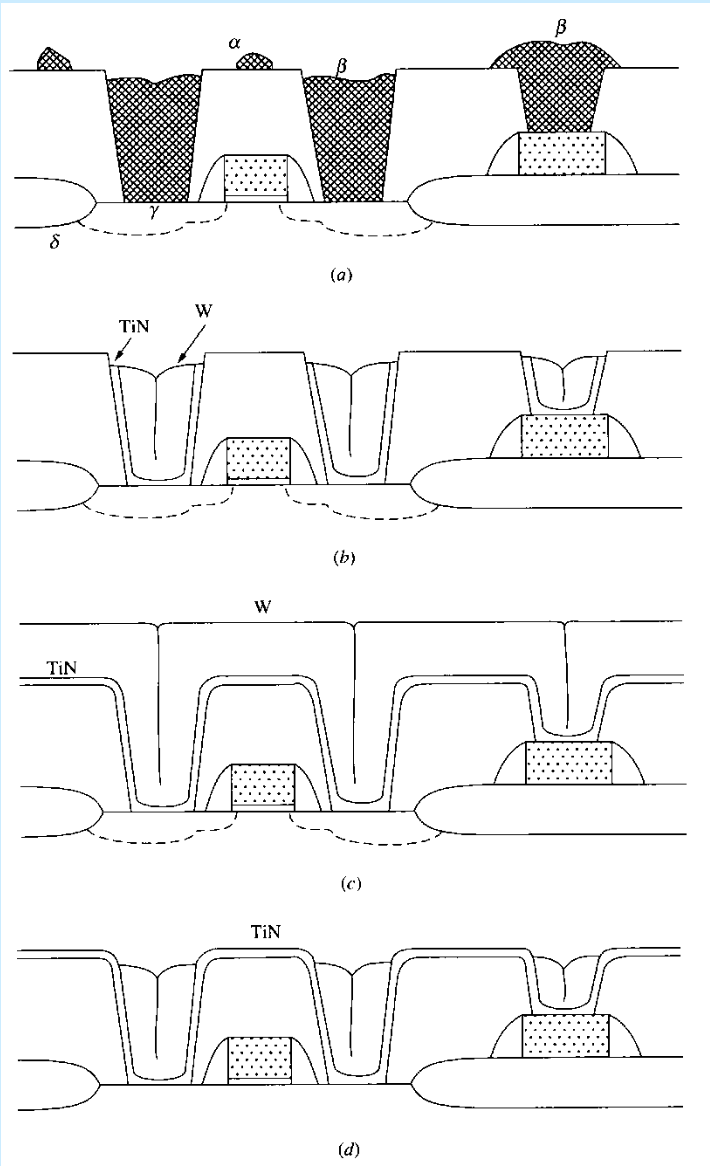
$$WF_6 + 3H_2 \rightarrow W + 6HF$$



The process does not have perfect selectivity, and as a result, spurious nucleation and W growth can occur on SiO_2 ***(a)***. Another factor that is unfavorable to a selective W plug process is the difficulty in filling contact windows of different heights. Since the contact to the gate is always shallower (by an amount equaling the gate height plus field oxide) than to the source / drain, selective W cannot fill both contact windows simultaneously. Hence, selective W is suitable only for via contacts.

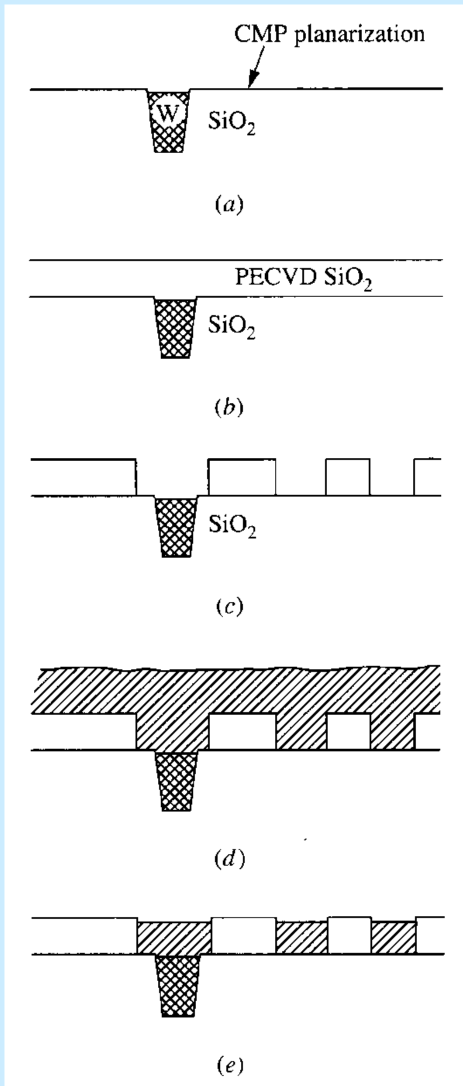


To improve the selectivity, a nucleation layer such as TiN can be deposited and then selectively removed from the SiO_2 area, leaving the layer only in the contacts ***(b)***. There are other advantages. It solves the different window height problem, because W grows from the sidewall as well as from the bottom of the contacts. The selectivity loss is less severe, since now the plug grows from the sidewall and much thinner W is needed. Finally, the adhesion of the W plug to the contact is better because of growth from the sidewall. This process shifts the difficulty of selective W deposition to the selective etching of TiN.

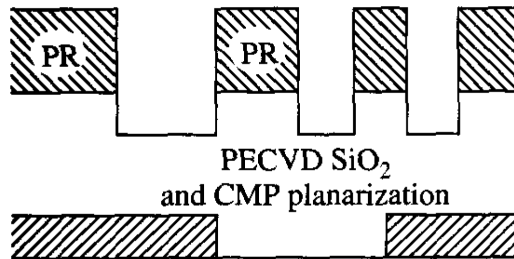


By depositing a metal nucleation layer such as TiN on the entire wafer, CVD W can be blanket deposited on the wafer and in the contact windows. The W on the SiO_2 is then etched away using RIE, leaving only the thicker W in the contact ***(c and d)***. Since this process relies on the removal of all CVD W except in the contacts, the uniformity of the W deposition and RIE etchback is critical for the control of the process.

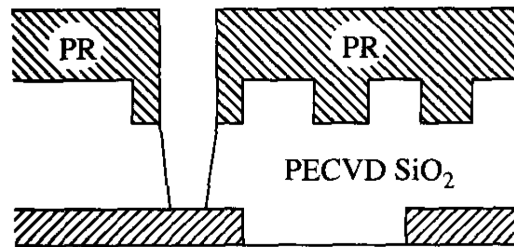
Damascene



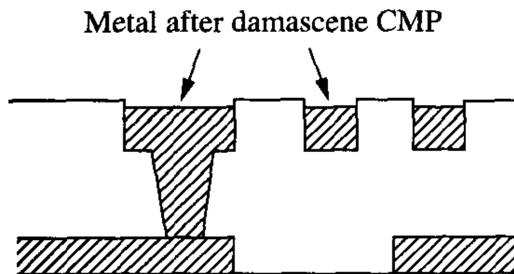
- The damascene process derives its name from the ancient art of the Middle East involving inlaying metal in ceramic or wood
- After the via plug process, the interlevel dielectric (ILD) is deposited without planarization
- Trenches for metal lines are defined, etched in the ILD ***(c)***, and filled with a metal such as copper ***(d)***
- The excess metal on the surface is removed to form a planar structure with metal inlays in the dielectric ***(e)***
- The damascene process eliminates the difficulty in filling small gaps between metal wires as well as in metal etching, especially for Cu and other hard-to-etch metals



(a)



(b)

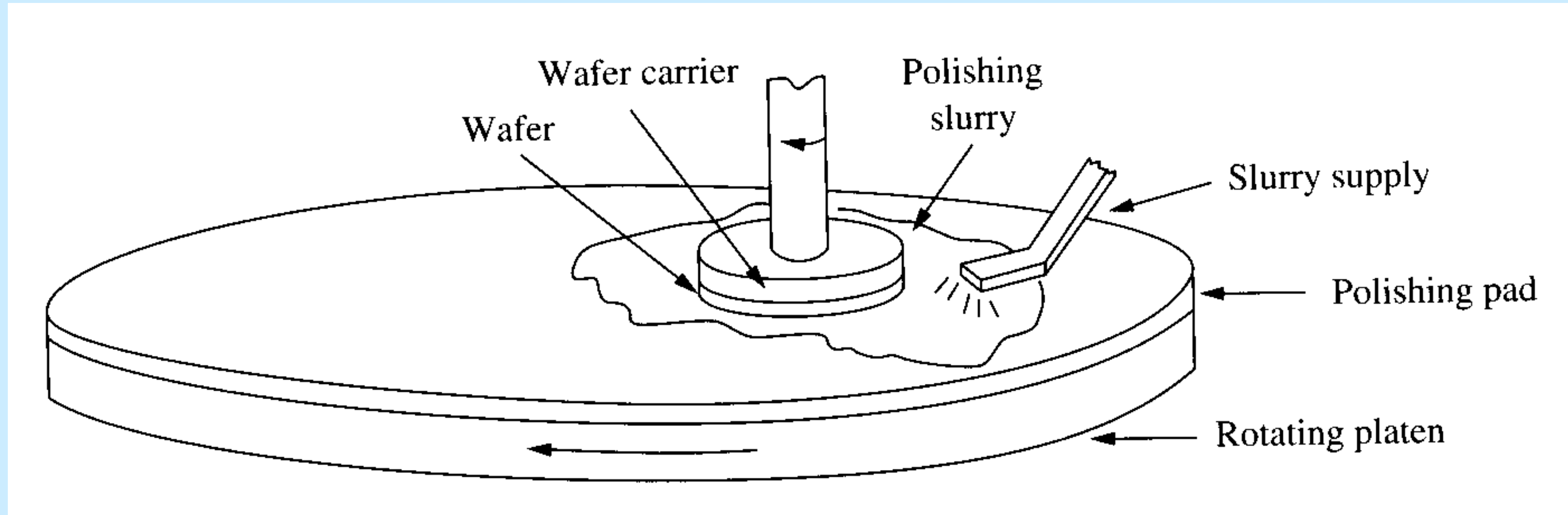


(c)

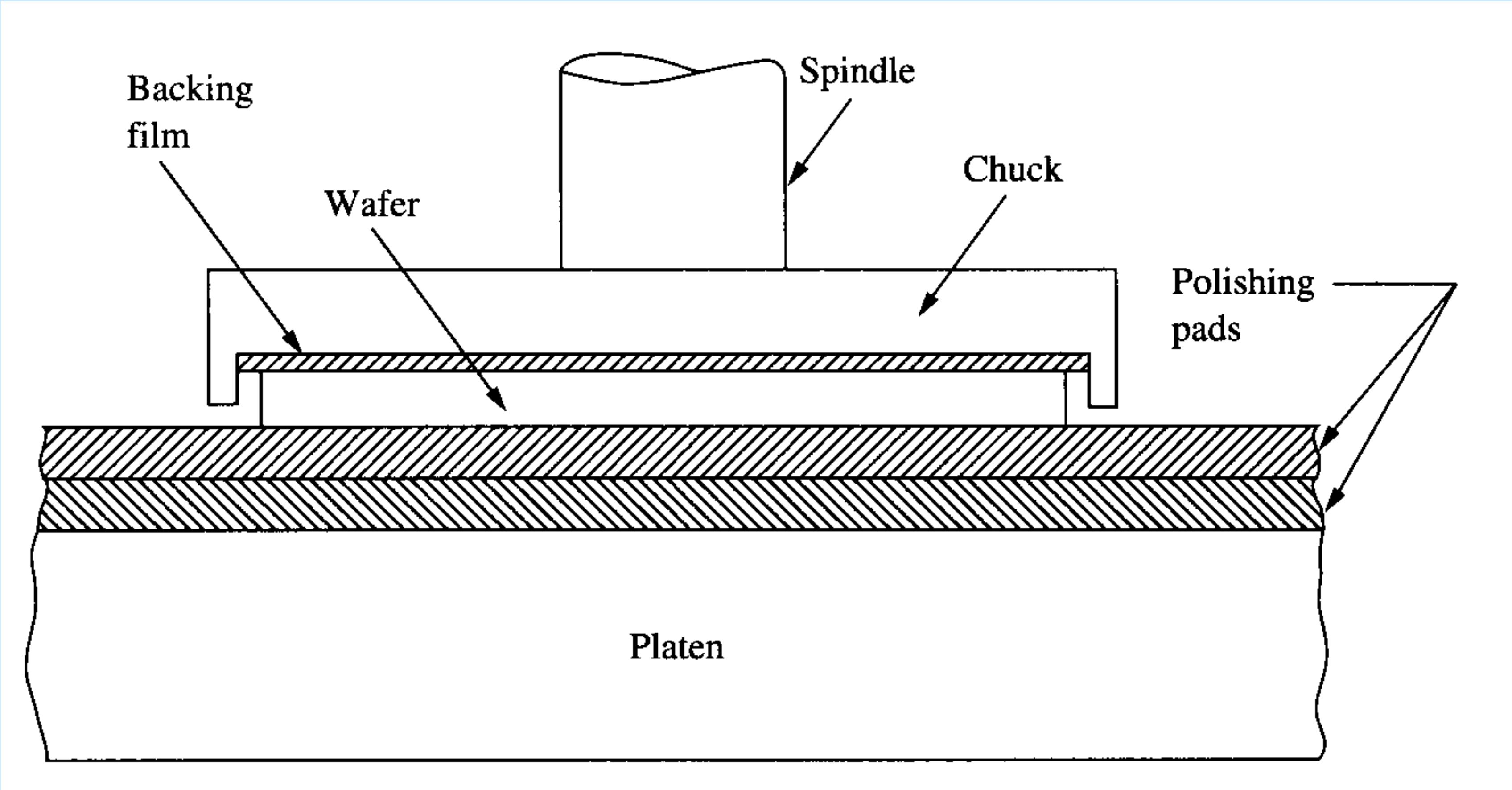
Dual Damascene

- In the dual damascene process, vias and trenches are defined using two lithographic and RIE steps
- The via plug is filled in the same step as the metal line ***(c)***
- Dual damascene minimizes the number of processing steps by reducing the barrier layer depositions from two to one and by eliminating the CVD W plug processes

Chemical Mechanical Polishing (CMP)



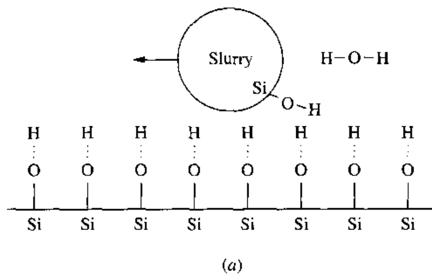
- Chemical mechanical polishing (CMP) is used to planarize the SiO_2 and metal
- The process is similar to that used to polish silicon wafers


Backing
film
Wafer
Spindle
Chuck
Polishing
pads
Platen

Even though CMP is essentially mechanical in nature, the microscopic action of polishing is both chemical and mechanical. The mechanical removal rate is given by the Preston equation:

$$R = K_p p v$$

where K_p is the proportionality constant depending on the mechanical properties of the materials being polished and the polishing pads as well as the polishing slurry, p is the applied pressure, and v is the relative velocity between the wafer and the polishing pad



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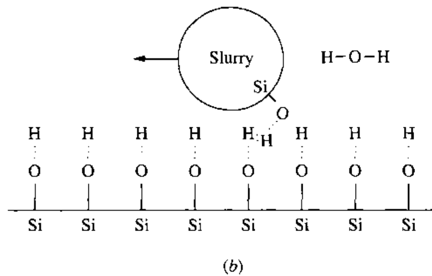

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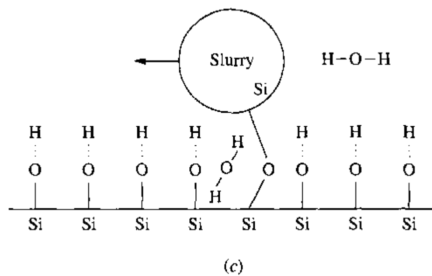
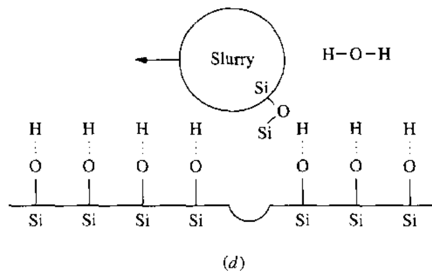


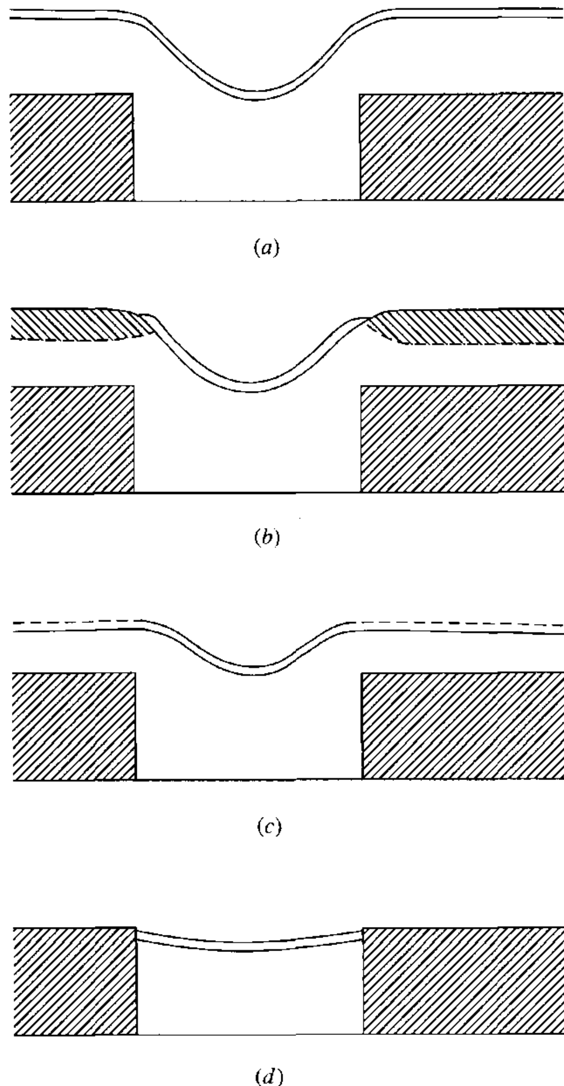
(c)



(d)

- Formation of hydrogen bonds with the oxide surfaces of both the wafer and the slurry particles (hydroxylation), as shown in ***(a)***
- Formation of hydrogen bonds between the wafer and the slurry ***(b)***
- Formation of molecular bonds between the wafer and slurry ***(c)***
- Breaking of the oxide bonds with the wafer (or the slurry) surface when the slurry particle moves away ***(d)***

Metal CMP



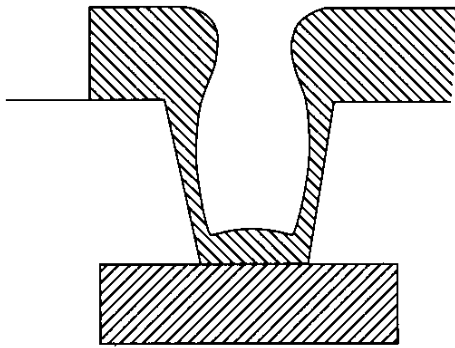
- The mechanism of CMP of metal is less understood and more complex than that of oxide polishing
- This example illustrates a metal polishing model employing both chemical etching and a passivation mechanism
- For metal CMP, the polishing slurry must contain three important constituents: the fine slurry particles, a corrosion (etching) agent, and an oxidant
- Planarization is achieved by the mechanical rigidity of the polishing pad similar to silicon polishing

CMP End Point Detection

- It is difficult to detect the end point of a CMP step as there is no clear signal about when the process has been completed
- Empirical polishing rates and timed polishing are used
- Better control can be achieved by installing an end point mechanism such as capacitive measurement and optical measurement

Contact Electromigration

- With multiple levels of wiring, it is necessary to pass current from one level of metal to another through vias
- When the metal design rules scale down, the size of the contact vias also shrinks accordingly, and the current density in the vias can be as high as, and sometimes even higher than, that in the metal conductors
- In practice, via electromigration has been observed for two reasons: (1) poor metal step coverage of the vias resulting in very high current density and (2) the use of different materials in the via (such as W plug) giving rise to localized current crowding and high current density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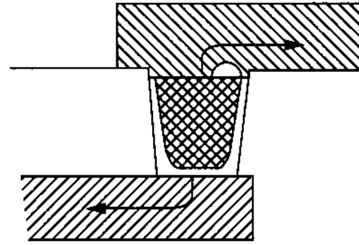
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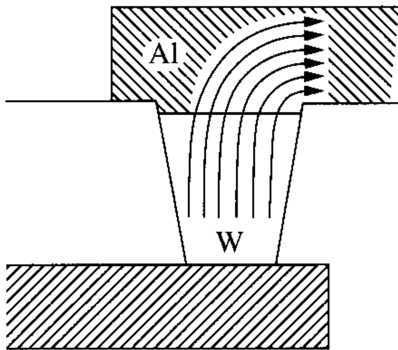
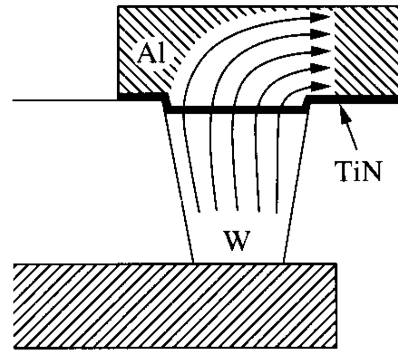
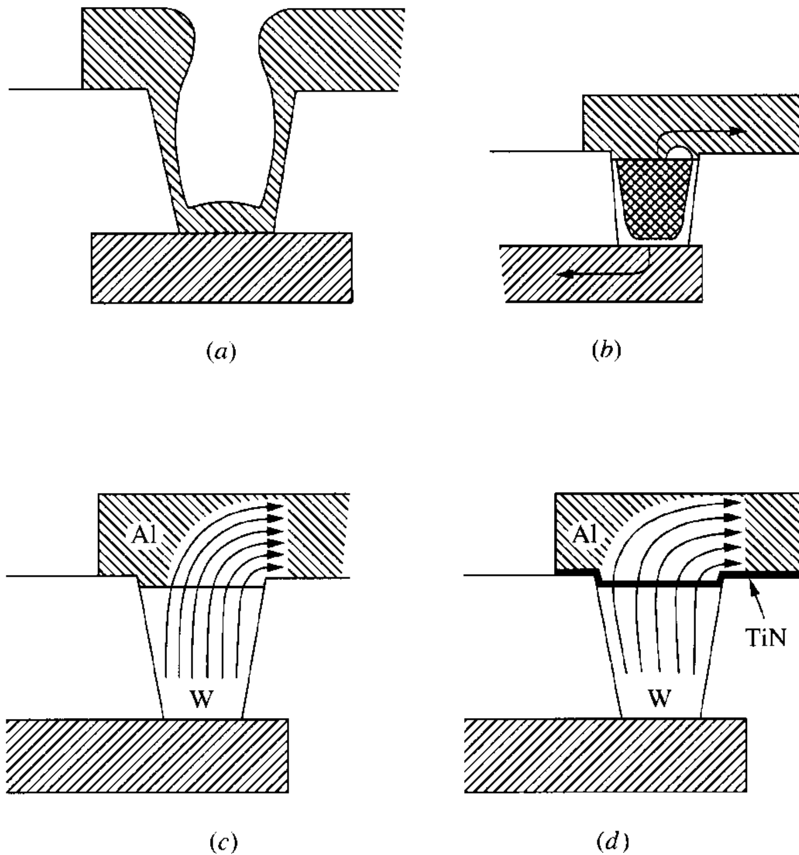


(c)



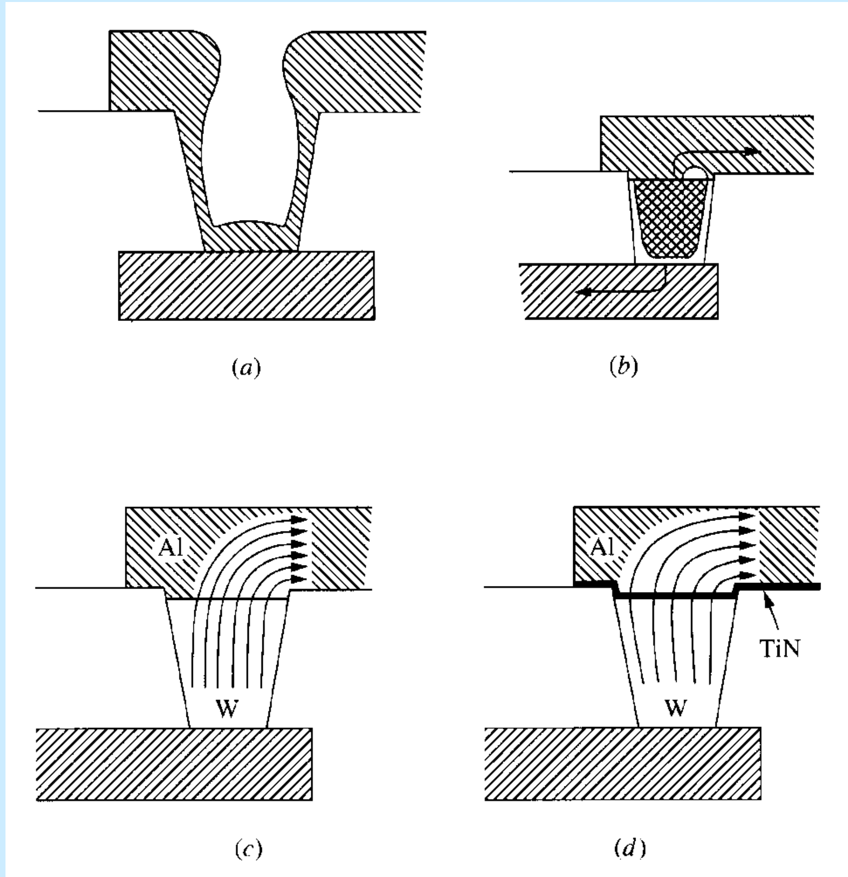
(d)

In ***(a)***, a typical contact via carries a current from a transistor. The current density in the via is much higher that of a fully filled via. This current density can be higher than the electromigration design limits and will cause early failure. This problem can be solved by using W or Al plugs



(b) illustrates electromigration induced voiding when a CVD W plug is used in a via and Al wiring is in direct contact with the W plug. Even so, current crowding may still occur when current goes through the plug and into the next level of Al wire. This happens because the via intersects the Al wire at a right angle, and the electrical current has to turn 90° when entering the Al wire.

Various current paths offer different resistances, and current tends to go through the least resistive path, that is, the inner corner as shown in ***(b)*** and ***(c)***. The phenomenon drives more current through the inner corner of the plug and the adjacent Al wire.



There are two approaches to mitigate electromigration voiding at the via contact: (1) replacing the W plug with an Al plug to ensure the continuity of the Al flux or (2) reducing the current density at the corner of the via contact. The second approach is illustrated in ***(d)***. By applying a layer of TiN between the W plug and the Al wire, the current overcrowding at the inner corner can be reduced as the TiN with higher electrical resistance helps distribute the current from the via to a wider area in the Al wire

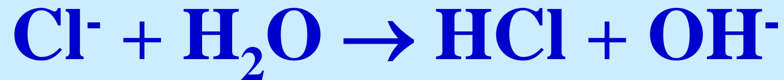
Metal Corrosion

- Aluminum grows a passivating oxide in air and is naturally protected against corrosion
- In order to increase electromigration resistance, aluminum wiring used in integrated circuits contains Cu which has no passivating oxide, and the Al-Cu alloy is thus more vulnerable to corrosion

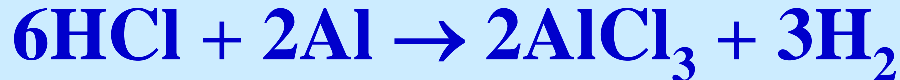
Corrosion of Al wires come from four sources

- Cl transported through the plastic packaging and passivation materials
- Cl from etching compound and etching by-products
- Phosphoric acid formed from excess P in phosphosilicate glass (PSG)
- Electrochemical (galvanic) corrosion from dissimilar materials

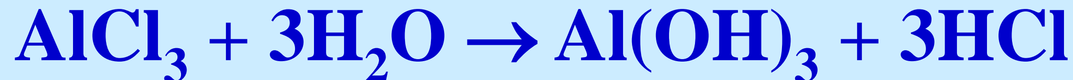
Chlorine plays an important role in the corrosion of Al through the following reactions



$$Cl^- + H_2O \rightarrow HCl + OH^-$$



$$6HCl + 2Al \rightarrow 2AlCl_3 + 3H_2$$



$$AlCl_3 + 3H_2O \rightarrow Al(OH)_3 + 3HCl$$

Note that the last two reactions are cyclical. After the initial formation of HCl, no additional Cl is required. The presence of the Cl ion is only to facilitate the net reaction:

$$2Al + 6H_2O \rightarrow 2Al(OH)_3 + 3H_2$$

- Since most chemicals used for Al dry etching or RIE contain chlorine, $AlCl_3$ or a similar compound is formed on the Al surface afterwards, and upon exposure to moisture in air, Al corrosion can be quite severe
- Careful cleaning is thus necessary after the etching step
- With regard to corrosion due to PSG, the average P content in PSG must not be too high (average P content below 6%)
- The reflow temperature can be lowered by adding a few percent of boron to the PSG

Modern metal structures use multilevels of dissimilar materials such as Ti / TiN / Al-Cu / TiN, and the chance of electrochemical corrosion is increased. For a W-plug / Al-wiring structure, Al is more electronegative than W. It can become the anode and be corroded:

$$Al \rightarrow Al^{3+} + 3e^{-} \qquad \text{(Anode: Al)}$$

$$2H^{+} + 2e^{-} \rightarrow H_2 \qquad \text{(Cathode: W)}$$

Copper is electropositive relative to hydrogen and is not vulnerable to electrochemical corrosion. However, in air copper oxide grows linearly with time, indicating the lack of a protective layer. Copper metallization thus requires the use of protective layers