CHAPTER 10: Metallization

Conductive films provide electrical interconnection among devices as well as the outside. ***Figure 10.1*** depicts the metallization scheme of a MOSFET. The primary metallization applications can be divided into three categories: gate, contact, and interconnection. Polysilicon and silicide are frequently used in gates and interconnects in MOS devices. Aluminum and copper are the metals of choice as contact and second-level interconnection to the outside. In some cases, a multiple-layer structure involving a diffusion barrier is used. Titanium / platinum / gold or titanium / palladium / gold is useful in providing reliable connection to external components. Some of the desired properties of metallization materials for VLSI are listed in ***Table 10.1***.

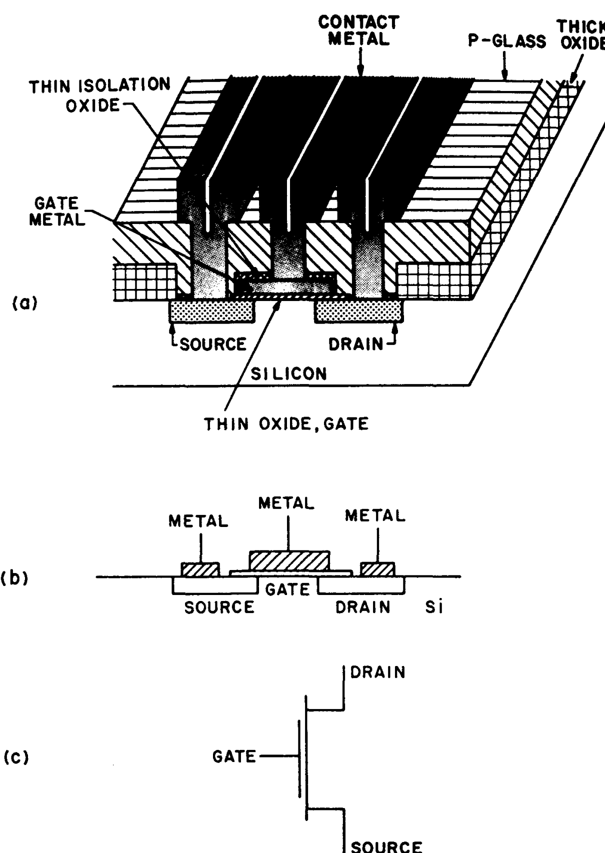

Figure 10.1: A typical MOSFET: (**a**) Three-dimensional cross section. (**b**) Schematic representation. (**c**) Circuit representation.

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Table 10.1: Desired properties of the metallization for integrated circuits.

1.	Low resistivity
2.	Easy to form
3.	Easy to etch for pattern generation
4.	Should be stable in oxidizing ambients and oxidizable
5.	Mechanical stability, good adherence, and low stress
6.	Surface smoothness
7.	Stability throughout processing, including high temperature sinter, dry or wet oxidation, gettering, phosphorus glass (or any other materials) passivation, and metallization
8.	No reaction with final metals
9.	Should not contaminate devices, wafers, or working apparatus
10.	Good device characteristics and lifetimes
11.	For window contacts - low contact resistance, minimal junction penetration, and low electromigration

In addition to providing contacts, gate and interconnection, metallization plays two important roles. The circuit speed is controlled by virtue of the resistance and capacitance of the interconnection runners. Moreover, it dictates the flat-band voltage V_{FB}:

$$V_{FB} = \phi_m - \phi_s \equiv \phi_{ms} \qquad \text{(Equation 10.1)}$$

where ϕ_m is the work function of the gate metallization and ϕ_s is the work function of the semiconductor. V_{FB} is the voltage required to counter balance the work function difference between the metal and semiconductor so that a flat-band condition is maintained in the semiconductor. V_{FB} thus contributes to the threshold voltage V_T which designates the voltage required at the gate metal to achieve conduction between the source and drain regions.

A good ohmic contact ought to be stable both electrically and mechanically, and the contact resistance R_C should be negligible. R_C is related to the Schottky barrier height of the metal ϕ_B and the dopant density N. The existence of a Schottky barrier between the metal and semiconductor stems from the requirement that the Fermi levels in the two materials must align at the interface. ***Figure 10.2*** depicts the relationship between R_C, ϕ_B, and N_D for contacts in an n-type silicon substrate. As shown, R_C diminishes with increasing dopant concentration and decreasing barrier height.

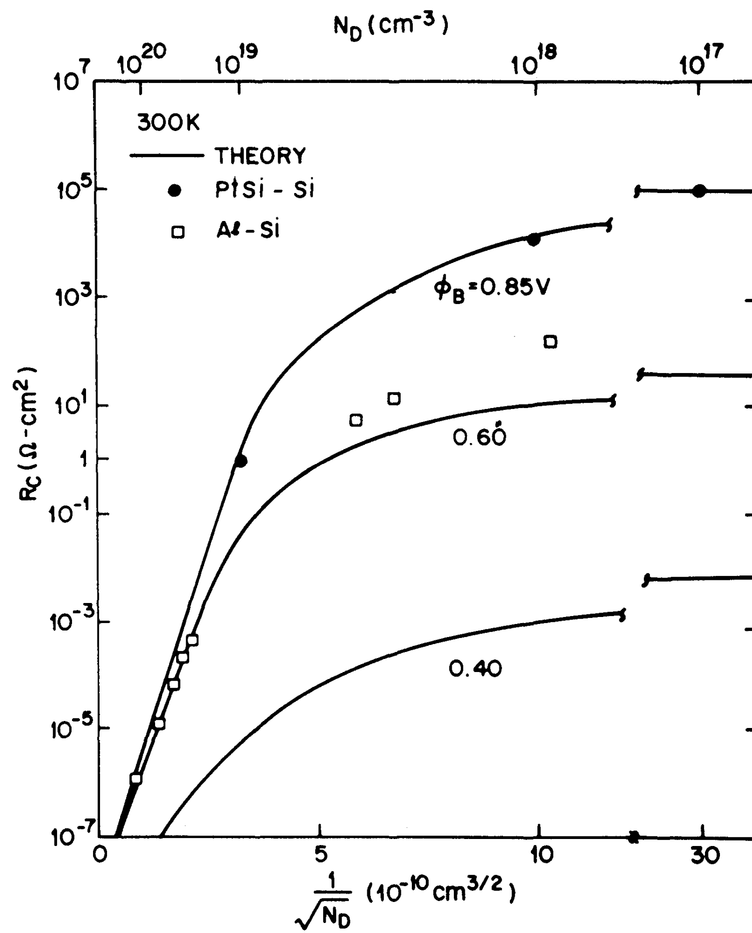


Figure 10.2: Theoretical and experimental values of contact resistance R_C as a function of the dopant concentration N_D and barrier height ϕ_B.

10.1 Metallization Choices

No metal satisfies all the desired characteristics tabulated in ***Table 10.1***. For example, even though aluminum possesses most of the desired properties, it suffers from a low melting point, spiking shorts, and electromigration. Polysilicon, refractory metal silicides ($MoSi_x$, $TaSi_x$, WSi_x, and $TiSi_x$), aluminum, and copper are used in gates and interconnects (***Table 10.2***).

Table 10.2: Possible metallization choices for integrated circuits.

Application	**Choices**
Gates and interconnection and contacts	Polysilicon, silicides, nitrides, copper, refractory metals, aluminum, and combinations of two or more of above
Diffusion barrier	Ti, TiN, Ta, TaN, Ti-W alloy, silicides
Top level	Aluminum, copper
Selectively formed metallization on silicon only	Some silicides, tungsten, aluminum, copper

Aluminum on silicon or silicide can lead to deleterious metallurgical interaction. Annealing of aluminum on silicon at 450°C causes dissolution of silicon into the metal and leads to pit formation. If this penetration is deep, contact and junction failure can result. A useful solution is to dope the Al with approximately 1 wt. % Si. This serves to reduce the diffusion of silicon from the underlying substrate. However, the problem is not totally circumvented if the contact is fabricated on n-type silicon, because the excess amount of silicon present in aluminum can, upon cooling, precipitate in the contact. This can lead to nonohmic contact to n-type silicon because the crystallized silicon precipitates contain aluminum which is a p-type dopant. In order to solve this problem, a diffusion barrier such as titanium nitride is applied between the aluminum metallization and the silicon substrate. Generally, a thickness on the order of 50 to 100 nm is sufficient.

Electromigration, which causes considerable material transport in metals, occurs because of enhanced and directional mobility of atoms under the influence of an electric field. Electromigration in aluminum is known to result in voids which

are manifested by discontinuities in the metallization runners and pileups that can short-circuit adjacent conductors. The electromigration resistance can be increased by alloying with copper (~ 0.5%).

Metallization is deposited by either physical vapor deposition (PVD) or chemical vapor deposition (CVD).

10.2 Physical Vapor Deposition

The most common forms of physical vapor deposition (PVD) are evaporation, e-beam evaporation, plasma spray deposition, and sputtering. Evaporation and e-beam evaporation used to be the workhorses in the IC industry but sputtering is now the dominant PVD technique in the industry. Sputtering has prevailed due to the following reasons:

(1) The high deposition rate afforded by modern cathode and target design.
(2) The capability to deposit and maintain complex alloy compositions.
(3) The ability to deposit high-temperature and refractory metals.
(4) The capability to maintain well-controlled, uniform deposition on large (200 mm and larger) wafers.
(5) The ability, in multi-chamber systems, to clean the contact before depositing metal.

Sputtering is usually carried out in an argon plasma. By biasing the target (source of metal) negatively, argon ions are attracted to the target. The momentum of the Ar ions is transferred to the target resulting in the ejection of one or more atoms from the surface of the target. The sputtered atoms, mostly neutral, fly into the plasma and land on the wafer. The angular distribution of the sputtered particles follows the cosine law. Therefore, like evaporation, sputter deposition occurs essentially along a line-of-sight path with a cosine distribution. Poor step coverage can result if the surface topography of the wafer is abrupt. The uniformity of the deposited film can be improved by raising the substrate temperature (enhancing surface migration), using a larger target, or inserting a collimator between the sputtering cathode and the wafer.

Reactive sputtering of TiN is conducted by introducing nitrogen into the Ar plasma in the sputtering chamber. The plasma provides enough energy to dissociate the nitrogen molecules into atomic nitrogen, which subsequently reacts with Ti to form TiN.

10.3 Chemical Vapor Deposition

Chemical vapor deposition (CVD) offers several advantages, of which three are particularly important:

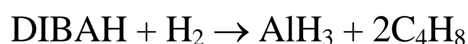
(1) Excellent step coverage.
(2) Large throughput.
(3) Low-temperature processing.

A number of metals and metal compounds, such as Al, Cu, WSi_2, TiN, and W, can be deposited by chemical reaction or thermal decomposition of precursors. The nature of metal CVD is not different from that of Si or SiO_2 CVD. A precursor chemical containing the desired metal and a chemical reaction or decomposition are the key ingredients. Usually the wafer needs to be heated to 100°C to 800°C to provide the initial thermal energy to overcome the reaction barrier. CVD metal can be deposited in a plasma. The advantage of plasma deposition is that the energy required to overcome the initial reaction barrier can be supplied by the plasma, and the deposition temperature can be decreased. This reduction is especially important for metal or metal compounds used for vias and multilevel interconnects since their tolerance for high temperature is limited.

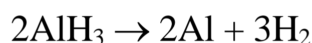
10.3.1 CVD Aluminum

Al can be deposited using several CVD precursors, such as tri-isobutyl-Al, $(C_4H_9)_3Al$, or TIBA. The chemistry involves a three-step decomposition process:

$$\text{TIBA} + H_2 \rightarrow \text{DIBAH} + C_4H_8$$



$$\text{DIBAH} + H_2 \rightarrow AlH_3 + 2C_4H_8$$



$$2AlH_3 \rightarrow 2Al + 3H_2$$

where DIBAH stands for di-isobutyl Al hydride or $(C_4H_9)_2AlH$. The first reaction is at 40°C to 50°C before the gas reaches the wafer. The second reaction occurs on the wafer with the wafer heated to 150°C to 300°C. In practice, DIBAH is the chemical precursor decomposing on the wafer surface. However, the direct use of DIBAH is impractical owing to its low vapor pressure and low deposition rate.

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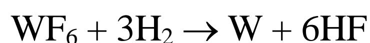
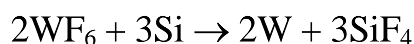
A problem with CVD Al is that there is no Cu in the materials to boost the electromigration resistance. A simple solution is to deposit ~50% of the total thickness of Al by CVD and the rest by sputtering of Al-Cu alloy. Subsequent heating to 250°C to 400°C allows the Cu in the alloy to redistribute to the entire Al wiring. Alternatively, CVD Al can be deposited with simultaneous Cu doping using dimethyl aluminum hydride (DMAH) and cyclopentadienyl copper triethylphosphine (CpCuTEP).

10.3.2 CVD Tungsten and Tungsten Silicide

The chemical vapor deposition of W and WSi_2 is widely practiced in integrated circuit fabrication. WSi_2 is used on top of gate polysilicon as a polycide structure and for local interconnects. CVD W is used both as a contact plug and first-level metal. The basic chemistry of CVD W is straightforward:

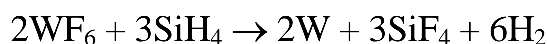


$$WF_6 + 3H_2 \rightarrow W + 6HF$$



$$2WF_6 + 3Si \rightarrow 2W + 3SiF_4$$

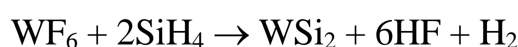
$$WF_6 + SiH_4 \rightarrow W + SiF_4 + 2HF + H_2$$



$$2WF_6 + 3SiH_4 \rightarrow 2W + 3SiF_4 + 6H_2$$

During CVD W deposition, the wafer is held on a heated chuck between 400°C and 500°C and opposite to an orifice where the WF_6, H_2, or SiH_4 gases are injected. Usually, a two- or three-step process is employed. SiH_4 is first introduced without WF_6 to initiate the deposition of a very thin layer (a few nanometers) of amorphous Si as a prenucleation layer. This is followed by a [SiH_4 + WF_6] silane reduction nucleation process and a high-rate [H_2 + WF_6] hydrogen reduction deposition. At the nucleation stage, less than 100 nm of W is deposited. The bulk of the W deposition is by hydrogen reduction.

WSi_2 is used widely on top of gate polysilicon to form a low-resistance polycide gate. CVD WSi_2 is readily deposited using the silane reduction of WF_6 at 300°C to 400°C:



$$WF_6 + 2SiH_4 \rightarrow WSi_2 + 6HF + H_2$$

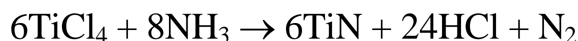
In a CVD reactor, the flow rates of WF_6 and SiH_4 control the outcome of the reaction. A higher SiH_4 to WF_6 ratio results in WSi_2 deposition. In practice, a ratio greater than 10 is used to ensure the deposition of WSi_x (x = 2.2 to 2.6).
WSi_2 can also be deposited by dichlorosilane (SiH_2Cl_2 or DCS) reduction at 500°C to 600°C:

$$2WF_6 + 7SiH_2Cl_2 \rightarrow 2WSi_2 + 3SiF_4 + 14HCl$$

$$2WF_6 + 7SiH_2Cl_2 \rightarrow 2WSi_2 + 3SiCl_4 + 12HF + 2HCl$$

10.3.3 CVD Titanium Nitride

TiN is widely used as a barrier metal layer for CVD W deposition and can be deposited by sputtering from a compound target or by reactive sputtering. CVD TiN can provide better coverage than PVD methods and is more economical than collimated sputtering. CVD TiN can be deposited using $TiCl_4$ and NH_3, H_2 / N_2, or NH_3 / H_2:



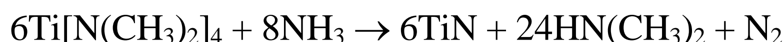
$$6TiCl_4 + 8NH_3 \rightarrow 6TiN + 24HCl + N_2$$

$$2TiCl_4 + 2NH_3 + H_2 \rightarrow 2TiN + 8HCl$$

$$2TiCl_4 + N_2 + 4H_2 \rightarrow 2TiN + 8HCl$$

The deposition temperature is 400°C to 700°C for NH_3 reduction and less than 700°C for the N_2 / H_2 reaction. Generally, the higher the deposition temperature, the better the TiN film and the less Cl incorporated into the TiN. However, even the best TiN produced by this process contains about 0.5% Cl. The lower temperature processes result in even higher Cl (~ 5%) causing concerns about the corrosion reliability of the Al wiring.

TiN can be deposited using metal-organic precursors that are usually in the form of a Ti-alkylamine complex. One example is the use of tetrakis-(dimethylamido)-Ti [also written as TDMAT or $Ti(NMe_2)_4$] and NH_3:

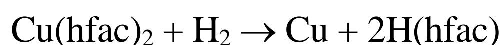


$$6Ti[N(CH_3)_2]_4 + 8NH_3 \rightarrow 6TiN + 24HN(CH_3)_2 + N_2$$

TiN deposition by metal-organic precursors can be done at low temperature ($\leq$ 450°C) and imposes no danger of Cl incorporation. However, C and O inclusion can give rise to high resistivity.

10.3.4 CVD Copper

Copper can be deposited by CVD readily. Because of its low resistivity and good electromigration resistance, Cu metallization is more desirable than Al in some applications. There are two types of metal-organic precursors for Cu: the divalent Cu^{II} in the form of Cu^{II}(β-diketonate)$_2$ and the monovalent Cu^{I} in the form of Cu^{I}(β-diketonate)L where L is a neutral ligand weakly bonded to Cu. The most commonly used Cu^{II} precusor is bis-hexafluoroacetyl-acetonate-Cu^{II} or Cu(hfac)$_2$. The structure $(CF_3COCHCF_3CO)_2Cu$ is shown in ***Figure 10.3***. High deposition rates and good quality films are achieved by hydrogen reduction:



$$Cu(hfac)_2 + H_2 \rightarrow Cu + 2H(hfac)$$

Although the [Cu(hfac)$_2$ + H_2] reaction starts at about 175°C, it does not reach the surface-reaction-limited stage until 320°C. Copper from Cu(hfac)$_2$ CVD can be deposited as blanket films or selectively.

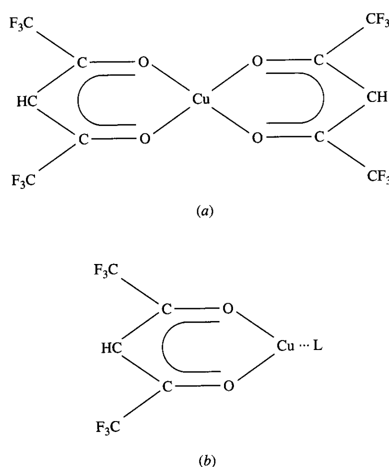


Figure 10.3: Molecular structures of (**a**) Cu^{II}(hfac)$_2$ and (**b**) Cu^{I}(hfac)L.

The structure of Cu^{I}(hfac)L is similar to that of Cu^{II}(hfac)$_2$, with the L ligand replacing one of the hfac rings. Examples of L are 2-butyne, vinyltrimethylsilane (vtms), and trimethylphosphine (PMe)$_3$. Depending on the L ligand, CVD using Cu^{I} compounds may be selective, blanket, or both. For example, Cu^{I}(hfac)(PMe)$_3$ is used to deposit Cu selectively only, but Cu^{I}(hfac)(2-butyne) deposits Cu only in a blanket fashion.

Copper lacks a dense oxide and is thus vulnerable to corrosion. Also, like Au, Cu can diffuse through SiO_2 and cause deep impurity levels in Si, reducing bipolar gain and causing junction leakage. In addition, Cu has no volatile compounds at room temperature and thus cannot be etched by the RIE process at moderate temperature ($\leq$ 200ºC). Therefore, the use of Cu as interconnects depends on issues well beyond the deposition techniques. To prevent corrosion and Cu diffusion into Si, a cladding layer such as TiN or Ta is needed.

10.4 Self-Aligned Silicide (Salicide)

A self-aligned silicide process has several advantages. The process does not require any additional lithography and etching, and alignment is pre-determined. It results in very clean silicon-silicide interfaces and consequently, highly reproducible contacts. ***Figure 10.4*** illustrates the processing steps for self-aligned gate, source, and drain silicide formation. In this sequence, polysilicon is first deposited on the gate oxide and doped. The oxide mask, Si_3N_4, is laid down using LPCVD process. The polysilicon-Si_3N_4 sandwich defines the gate and interconnection pattern. The source and drain are fabricated by ion implantation, followed by stripping of the photoresist. Oxidation is subsequently carried out to form oxide walls on the polysilicon (the nitride inhibits oxidation on the gate surface). After a heat treatment activates and diffuses the dopants, the oxide is removed anisotropically from the source and drain, leaving oxide sidewalls on the polysilicon. The remaining nitride is removed by selective chemical or dry etching leaving exposed polysilicon and source / drain surfaces. Titanium or cobalt is then deposited following an in-situ surface cleaning. After a silicide is formed by annealing, the unreacted metal is stripped by selective chemical etching, leaving behind silicide at the gate, source, and drain, and on the interconnection lines.

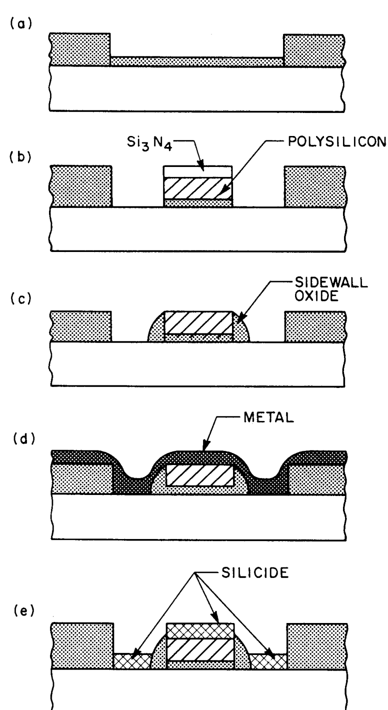
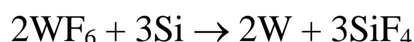


Figure 10.4: Process steps for self-aligned gate, source, and drain silicide formation.

10.5 CVD Tungsten Plug

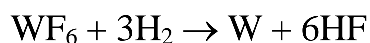
One of the difficult problems in metallization is to ensure enough metal continuity at contact windows and vias. The step coverage of sputtered Al degrades rapidly with increasing contact window aspect ratio, and at small design rules, the step coverage at contacts and vias drops below 20%. Consequently, various forms of metal plugs have been developed.

The selective CVD W plug process starts on a Si contact from a Si reduction process:



$$2WF_6 + 3Si \rightarrow 2W + 3SiF_4$$

This process provides a nucleation layer of W grown on Si but not on SiO_2. The real W plug is grown by the following hydrogen reduction process that deposits W rapidly on the nucleation layer:



$$WF_6 + 3H_2 \rightarrow W + 6HF$$

This process, however, does not have perfect selectivity, and as a result, spurious nucleation and W growth can occur on SiO_2 (***Figure 10.5a***). Another factor that is unfavorable to a selective W plug process is the difficulty in filling contact windows of different heights (***Figure 10.5a***). Since the contact to the gate is always shallower (by an amount equaling the gate height plus field oxide) than to the source / drain, selective W cannot fill both contact windows simultaneously. Hence, selective W is suitable only for via contacts.

To improve the selectivity, a nucleation layer such as TiN can be deposited and then selectively removed from the SiO_2 area, leaving the layer only in the contacts, as shown in ***Figure 10.5b***. There are other advantages. Firstly, it solves the different window height problem, because W grows from the sidewall as well as from the bottom of the contacts. Secondly, the selectivity loss is less severe, since now the plug grows from the sidewall and much thinner W is needed. Finally, the adhesion of the W plug to the contact is better because of growth from the sidewall. This process, however, shifts the difficulty of selective W deposition to the selective etching of TiN. The alternative is a blanket W-plug process.

By depositing a metal nucleation layer such as TiN on the entire wafer, CVD W can be blanket deposited on the wafer and in the contact windows. The W on the SiO_2 is then etched away using RIE, leaving only the thicker W in the

contact as shown in ***Figures 10.5c*** and ***10.5d***. Since this process relies on the removal of all CVD W except in the contacts, the uniformity of the W deposition and RIE etchback is critical for the control of the process.

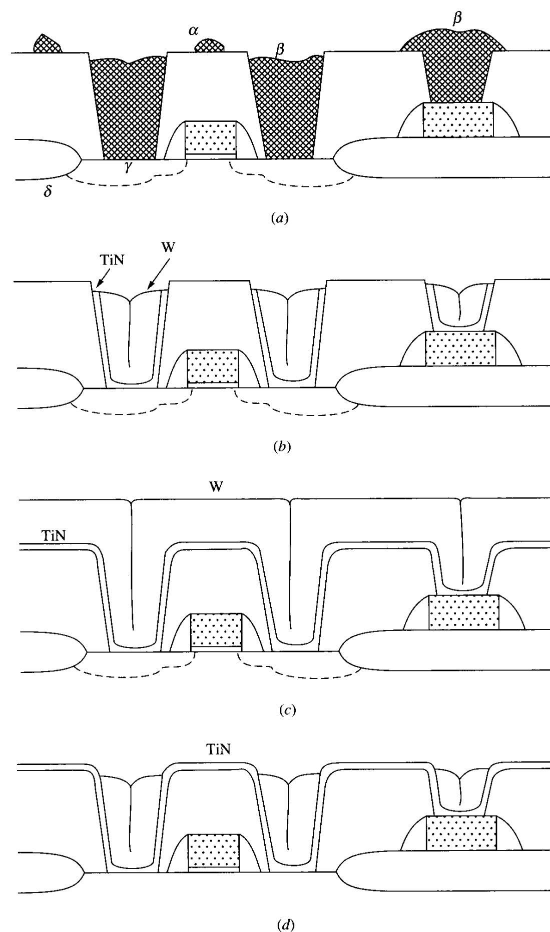


Figure 10.5: CVD W plug process: (**a**) Selective W with no barrier layer showing loss of selectivity (α), uneven hill (β), junction leakage (γ), and wormholes (δ). (**b**) Selective W with barrier liner without the problems shown in (a) but liners are hard to form. (**c**) Blanket deposition of W on TiN barrier. (**d**) After W etchback to form W plugs.

10.6 Damascene, Dual Damascene, and Chemical Mechanical Polishing

The damascene process derives its name from the ancient art of the Middle East involving inlaying metal in ceramic or wood for decoration. In IC manufacturing, a damascene process refers to a similar structure, as shown in ***Figure 10.6***. After the via plug process, the interlevel dielectric (ILD) is deposited without planarization, since the surface is already flat. Trenches for metal lines are then defined, etched in the ILD (***Figure 10.6c***), and filled with a metal such as copper (***Figure 10.6d***). The excess metal on the surface is removed and a planar structure with metal inlays in the dielectric is achieved (***Figure 10.6e***). The damascene process eliminates the difficulty in filling small gaps between metal wires as well as in metal etching, especially for Cu and other hard-to-etch metals.

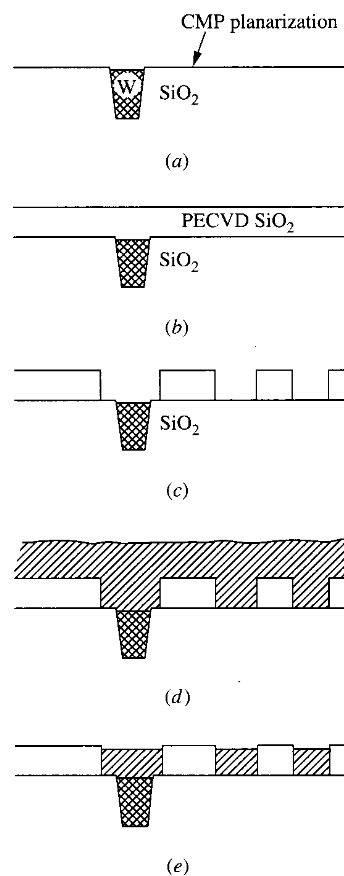


Figure 10.6: Damascene process: (**a**) Formation of metal plug after planarization of SiO_2 by CMP. (**b**) PECVD SiO_2 ILD deposition. (**c**) Trench patterning and RIE for metal lines. (**d**) Metal deposition to fill trenches. (**e**) Metal CMP to complete metal definition.

A dual damascene process is demonstrated in ***Figure 10.7***. In this process, vias and trenches are defined using two lithographic and RIE steps, but the via plug is filled in the same step as the metal line, as shown in ***Figure 10.7c***. Dual damascene minimizes the number of processing steps by reducing the barrier layer depositions from two to one and by eliminating the CVD W plug processes.

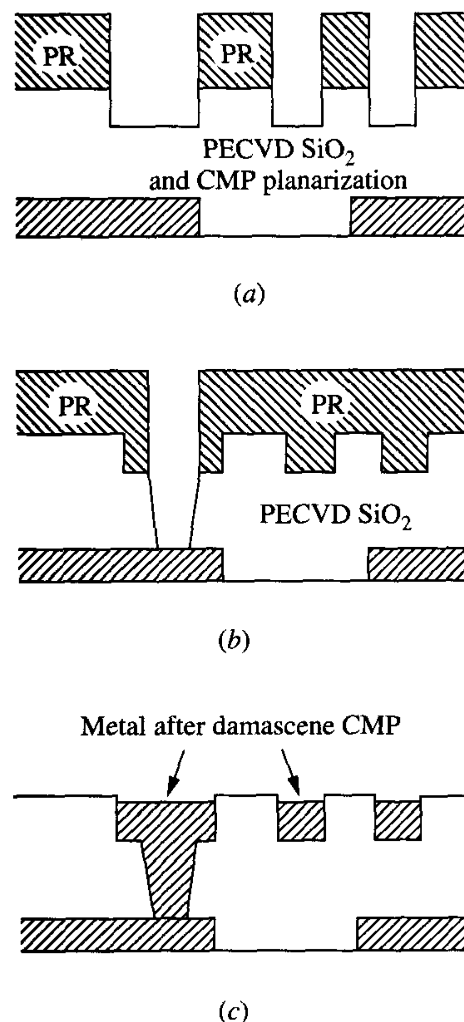


Figure 10.7: Dual damascene process: (**a**) Trench patterning after ILD planarization. (**b**) Stripping photoresist (PR), applying new PR, defining via pattern, and via RIE. (**c**) Metal deposition in both vias and trenches, and CMP to remove excess metal. Note that the via plug is of the same material as the upper-level metal in this process.

As shown in ***Figure 10.6*** and ***Figure 10.7***, a process called chemical mechanical polishing (CMP) is used to planarize the SiO_2 and metal. The process is similar to that used to polish silicon wafers. ***Figure 10.8*** depicts the schematic of a CMP polisher whereas the details of the CMP wafer carrier and polishing pads are exhibited in ***Figure 10.9***.

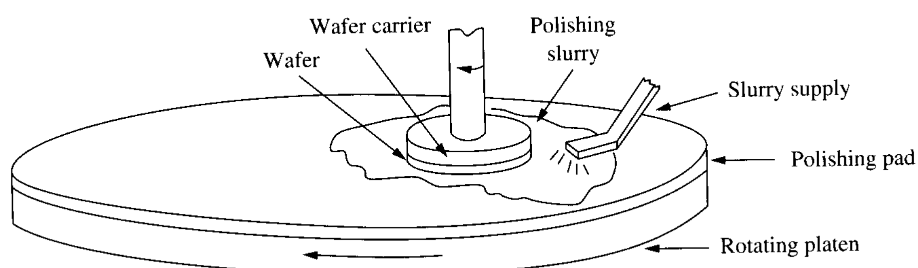


Figure 10.8: Schematic of a CMP machine.

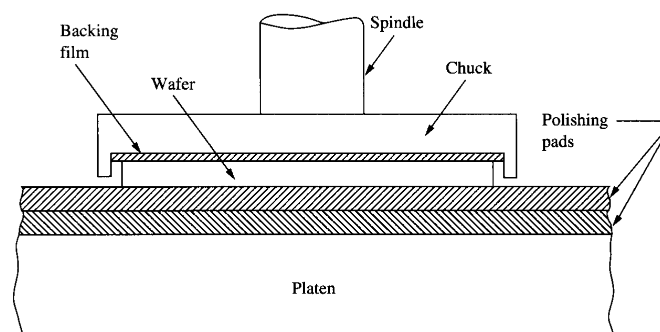


Figure 10.9: Details of the CMP wafer carrier and poishing pads.

Even though CMP is essentially mechanical in nature, the microscopic action of polishing is both chemical and mechanical. The mechanical removal rate is given by the Preston equation:

$$R = K_p pv \qquad \text{(Equation 10.2)}$$

where K_p is the proportionality constant depending on the mechanical properties of the materials being polished and the polishing pads as well as the polishing slurry, p is the applied pressure, and v is the relative velocity between the wafer and the polishing pad. ***Figure 10.10*** shows the chemical and mechanical events

during polishing of silicon. The chemical reactions can be divided into four stages:

(a) Formation of hydrogen bonds with the oxide surfaces of both the wafer and the slurry particles (hydroxylation), as shown in ***Figure 10.10a***.

(b) Formation of hydrogen bonds between the wafer and the slurry (***Figure 10.10b***).

(c) Formation of molecular bonds between the wafer and slurry (***Figure 10.10c***).

(d) Breaking of the oxide bonds with the wafer (or the slurry) surface when the slurry particle moves away (***Figure 10.10d***).

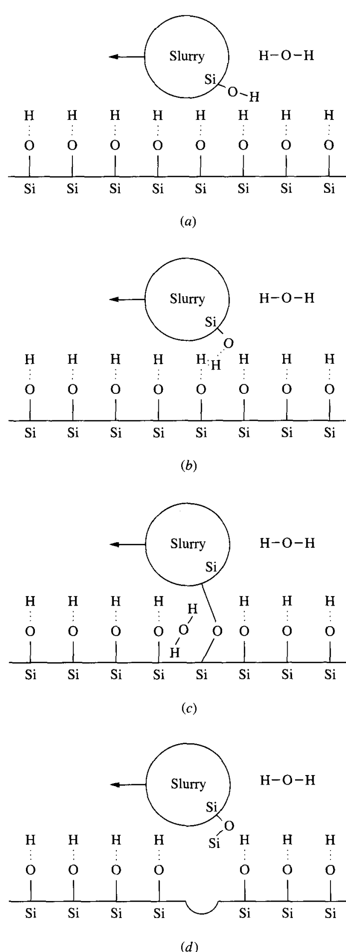


Figure 10.10: Mechanism of chemical mechanical polishing (CMP): (**a**) In aqueous solution, oxide forms hydroxyls. (**b**) Hydrogen bond is formed between the slurry particle and wafer. (**c**) Si-O bonds are formed by releasing a water molecule. (**d**) Si-Si bond breaks when the slurry particle moves away.

A combination of chemical and mechanical actions avoids mechanically damaged surface layer, and the microscopic nature of CMP distinguishes it from mechanical abrasion.

The mechanism of CMP of metal is less understood and more complex than that of oxide polishing. ***Figure 10.11*** illustrates a metal polishing model employing both chemical etching and a passivation mechanism. For metal CMP, the polishing slurry must contain three important constituents: the fine slurry particles, a corrosion (etching) agent, and an oxidant. Planarization is achieved by the mechanical rigidity of the polishing pad similar to silicon polishing.

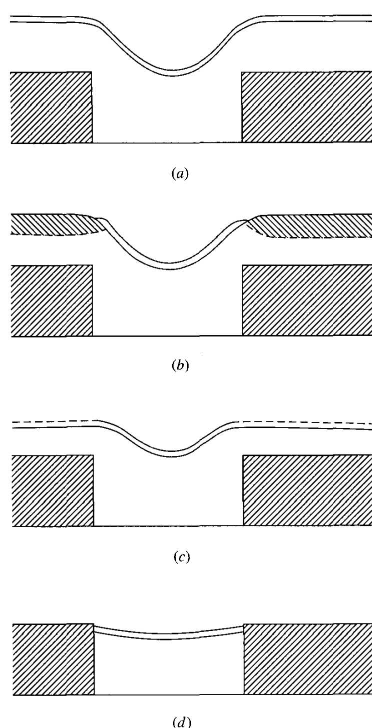


Figure 10.11: Mechanism of metal CMP: (**a**) Free metal surface is covered by a passivation oxide. (**b**) Oxide on the high spots is removed by CMP and metal is etched by the solution (shaded area). (**c**) Regrowth of oxide. (**d**) Processes illustrated in (b) and (c) are repeated until no high spot is left.

It is difficult to detect the end point of a CMP step as there is no clear signal about when the process has been completed. Consequently, empirical polishing rates and timed polishing are used. Better control can be achieved by installing an end point mechanism such as capacitive measurement and optical measurement.

10.7 Contact Electromigration

With multiple levels of wiring, it is necessary to pass current from one level of metal to another through vias. When the metal design rules scale down, the size of the contact vias also shrinks accordingly, and the current density in the vias can be as high as, and sometimes even higher than, that in the metal conductors. In practice, via electromigration has been observed for two reasons: (1) poor metal step coverage of the vias resulting in very high current density and (2) the use of different materials in the via (such as W plug) giving rise to localized current crowding and high current density.

The first case is elucidated in ***Figure 10.12a***. Consider a typical contact via carrying a current from a transistor. The current density in the via is much higher that of a fully filled via. This current density can be higher than the electromigration design limits and will cause early failure. This problem can be solved by using W or Al plugs.

Figure 10.12b illustrated the electromigration-induced voiding when a CVD W plug is used in a via and Al wiring is in direct contact with the W plug. Even with a plug in the via, current crowding still occurs when current goes through the plug and into the next level of Al wire. This happens because the via intersects the Al wire at a right angle, and the electrical current has to turn 90° when entering the Al wire. As a result, various current paths offer different resistances, and current tends to go through the least resistive path, that is, the inner corner as shown in ***Figure 10.12b*** and ***Figure 10.12c***. The phenomenon drives more current through the inner corner of the plug and the adjacent Al wire.

If the plug is made of Al, no void will form since the Al flux leaving the high-current spot will be compensated by Al flux from inside the plug and from Al farther up the line. For a W plug, however, there is no Al flux coming from the plug to replenish the Al flux leaving the hot spot. Consequently, voids will develop at the inner corner.

There are two approaches to mitigate electromigration voiding at the via contact: (1) replacing the W plug with an Al plug to ensure the continuity of the Al flux or (2) reducing the current density at the corner of the via contact. The second approach is illustrated in ***Figure 10.12d***. By applying a layer of TiN between the W plug and the Al wire, the current overcrowding at the inner corner can be reduced as the TiN with higher electrical resistance helps distribute the current from the via to a wider area in the Al wire.

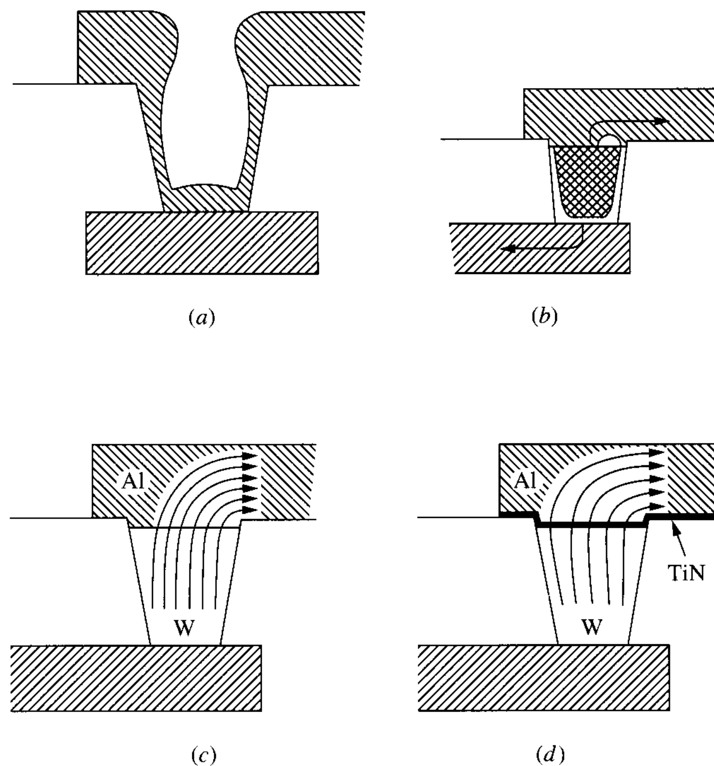


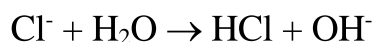
Figure 10.12: Contact electromigration: (**a**) Poor Al step coverage can cause high current density and Joule heating. (**b**) Al/W-plug contacts cause voiding at the corner of the Al/plug interface. (**c**) Current crowding occurs at the inner corner of an Al/W-plug contact. (**d**) Adding a TiN layer between the W plug and Al wire reduces the current crowding.

10.8 Metal Corrosion

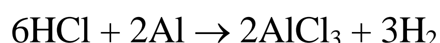
Aluminum grows a passivating oxide in air and is naturally protected against corrosion. However, in order to increase electromigration resistance, aluminum wiring used in integrated circuits contains Cu which has no passivating oxide, and the Al-Cu alloy is thus more vulnerable to corrosion. The corrosion of Al wires come from four sources:

(1) Cl transported through the plastic packaging and passivation materials.
(2) Cl from etching compound and etching by-products.
(3) Phosphoric acid formed from excess P in phosphosilicate glass (PSG).
(4) Electrochemical (galvanic) corrosion from dissimilar materials.

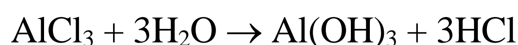
Chlorine plays an important role in the corrosion of Al through the following reactions:



$$Cl^- + H_2O \rightarrow HCl + OH^-$$

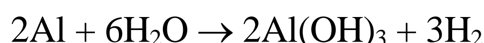


$$6HCl + 2Al \rightarrow 2AlCl_3 + 3H_2$$



$$AlCl_3 + 3H_2O \rightarrow Al(OH)_3 + 3HCl$$

Note that the last two reactions are cyclical. After the initial formation of HCl, no additional Cl is required. The presence of the Cl ion is only to facilitate the net reaction:



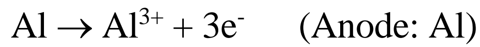
$$2Al + 6H_2O \rightarrow 2Al(OH)_3 + 3H_2$$

Hence, only a small amount of Cl is needed to cause severe local corrosion of the Al lines as the Cl^- ions recycle themselves during the corrosion process.

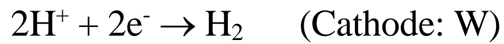
Since most chemicals used for Al dry etching or RIE contain chlorine, $AlCl_3$ or a similar compound is formed on the Al surface afterwards, and upon exposure to moisture in air, Al corrosion can be quite severe. Careful cleaning is thus necessary after the etching step. With regard to corrosion due to PSG, the average P content in PSG must not be too high (average P content below 6%). The reflow temperature can be lowered by adding a few percent of boron to the PSG.

Modern metal structures use multilevels of dissimilar materials such as Ti / TiN / Al-Cu / TiN, and the chance of electrochemical corrosion is increased. For

instance, for a W-plug / Al-wiring structure, Al is more electronegative than W. It can become the anode and be corroded:



$$Al \rightarrow Al^{3+} + 3e^{-} \qquad \text{(Anode: Al)}$$



$$2H^{+} + 2e^{-} \rightarrow H_2 \qquad \text{(Cathode: W)}$$

Copper is electropositive relative to hydrogen and is not vulnerable to electrochemical corrosion. However, in air copper oxide grows linearly with time, indicating the lack of a protective layer. Copper metallization thus requires the use of protective layers.